

MS-7733

Ver: 3.0

Mini ITX

Intel -MahoBay plamform

CPU:

INTEL-Ivy bridge LGA1155

System Chipset:

INTEL-Panther Point

OnBoard Chipset:

HD Audio Codec:RTL887

LAN-RTL8111E Co-lay 8105E

SIO:Fintek F171808A

Flash ROM: 64 Mb SPI (CHIP)

Main Memory:

SO-DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PWM:

VRD12 - UT501+3Phase

ACPI:

UPI

Other:

SATA(SATA2-300MB/s*3 + SATA3-500MB/s *1)

Rear USB2.0 *4+ Front USB2.0*4

REAL USB3.0 *2

FRONT USB3.0 *2

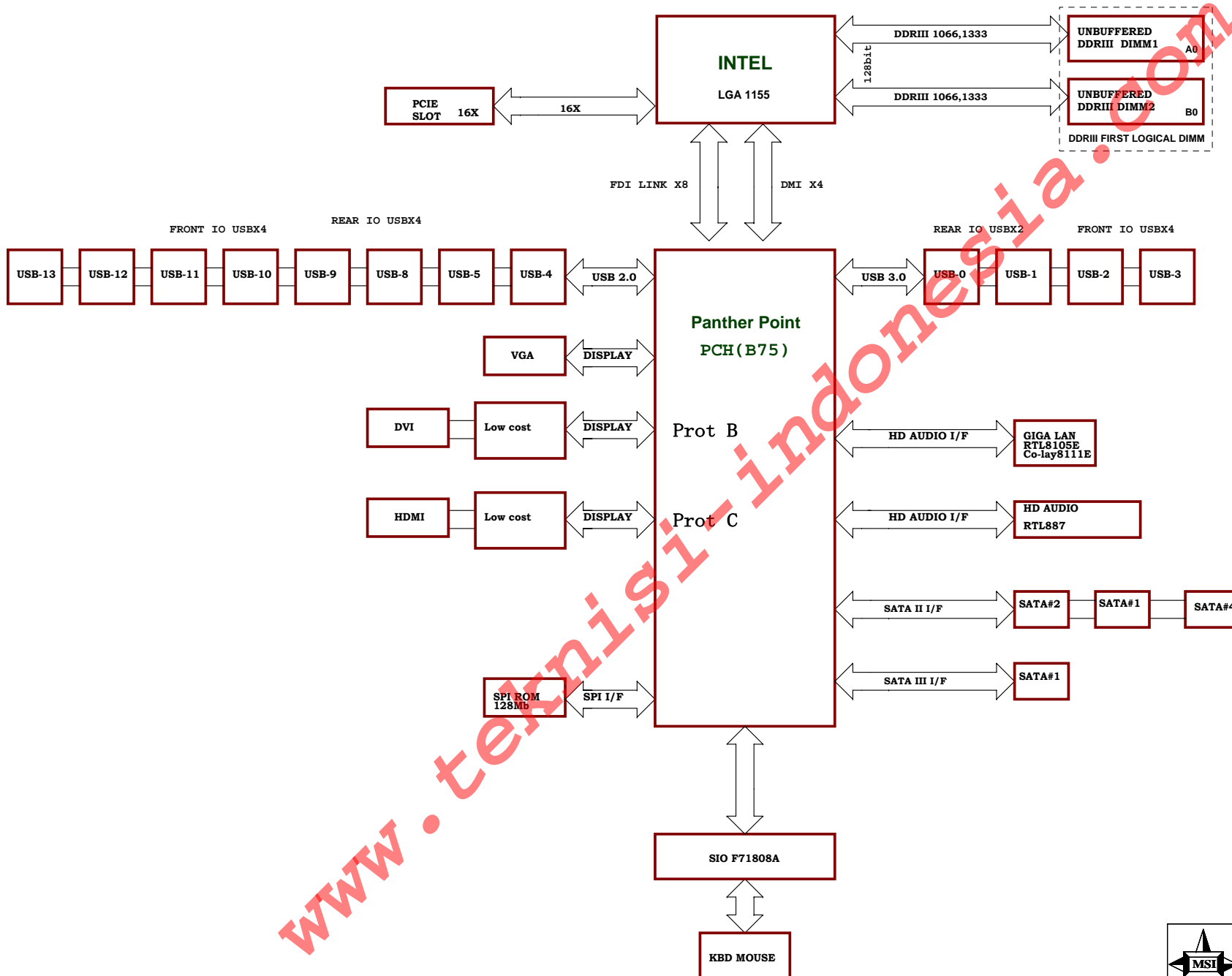
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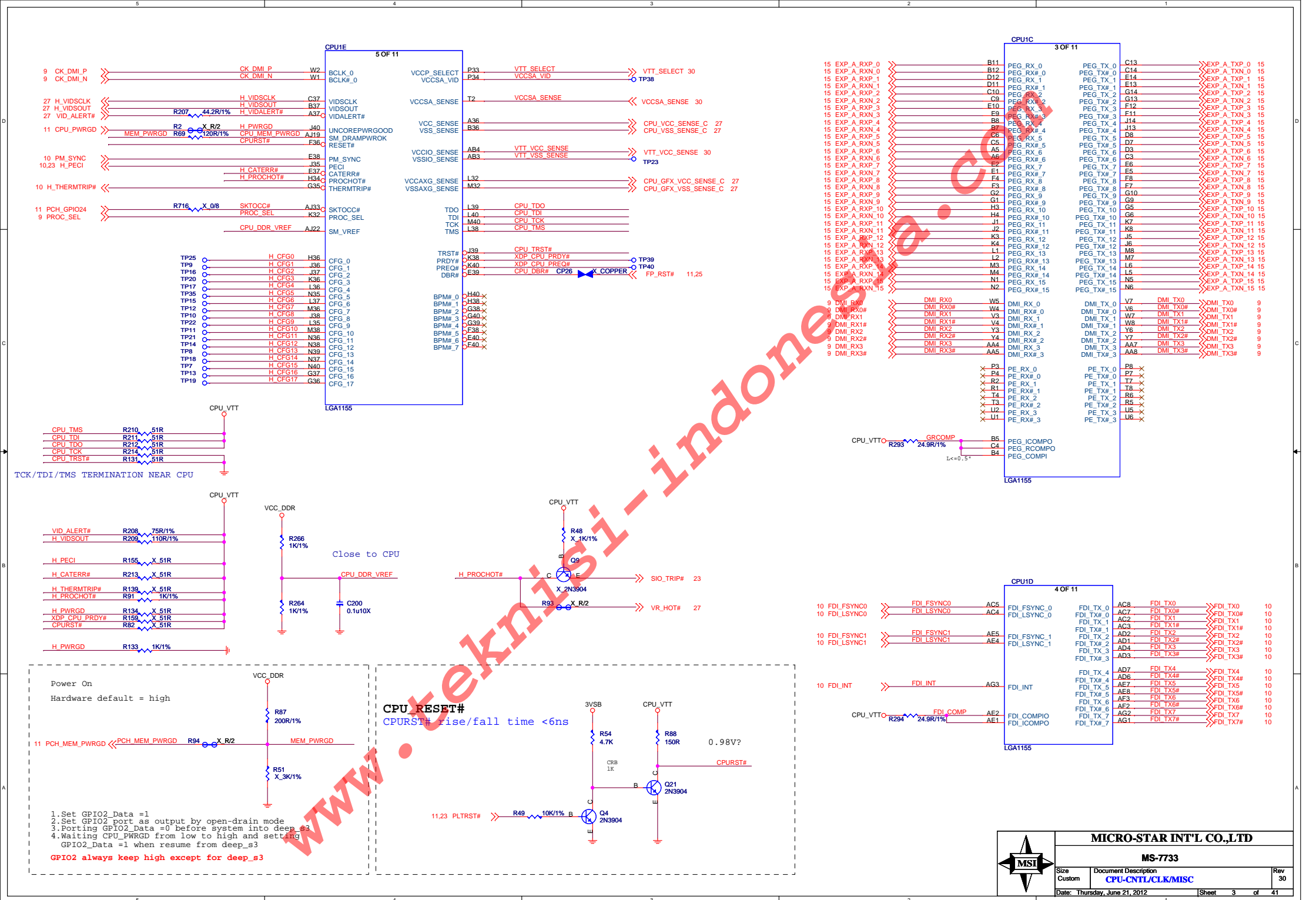


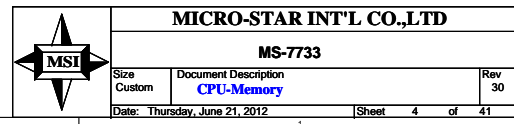
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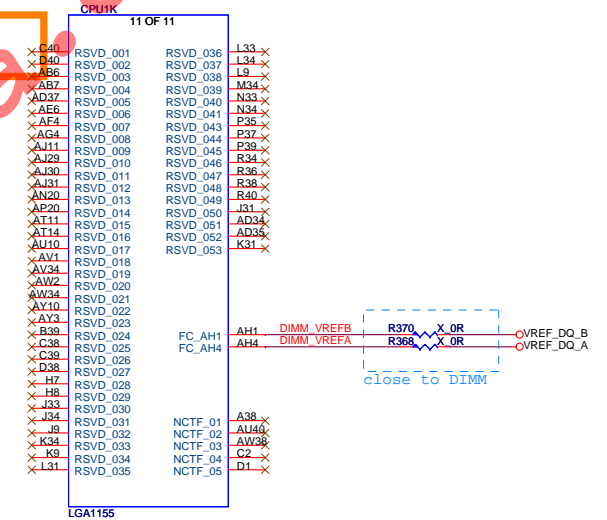
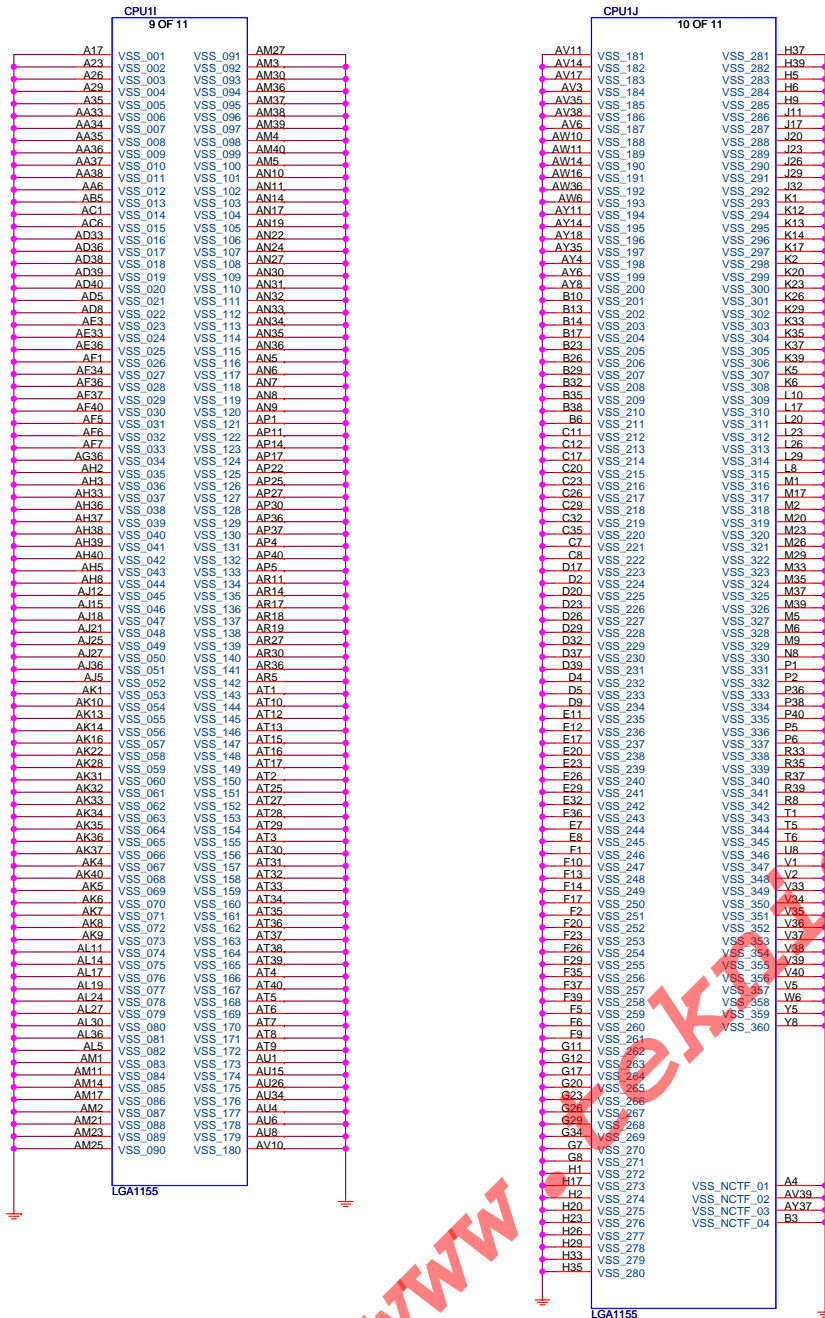
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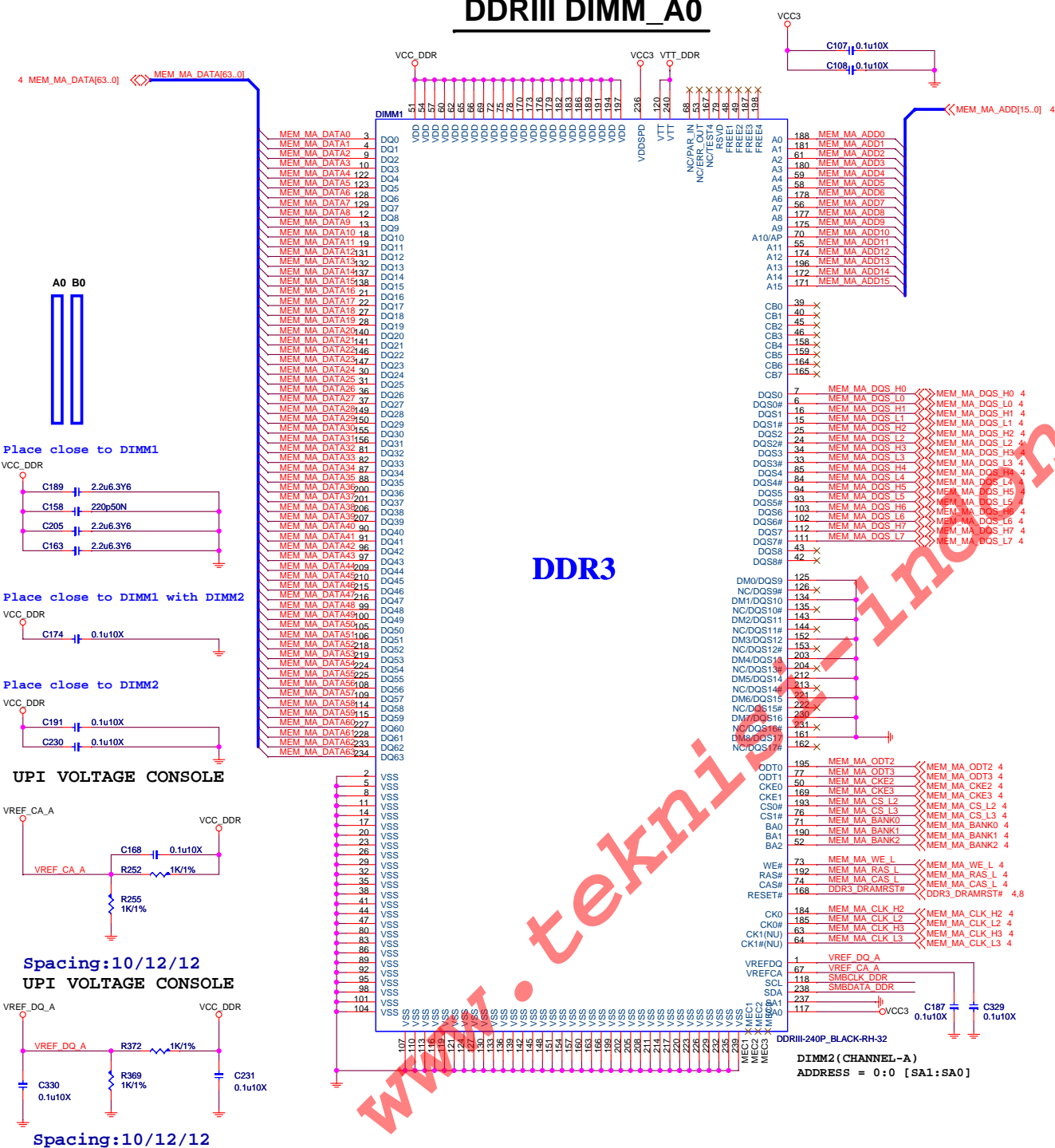




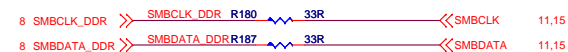




DDRIII DIMM_A0



```
VCC_DDR 2DIMM:5.5A
VTT_DDR 2DIMM:1A
VCC3.3: Min 40mil width
```

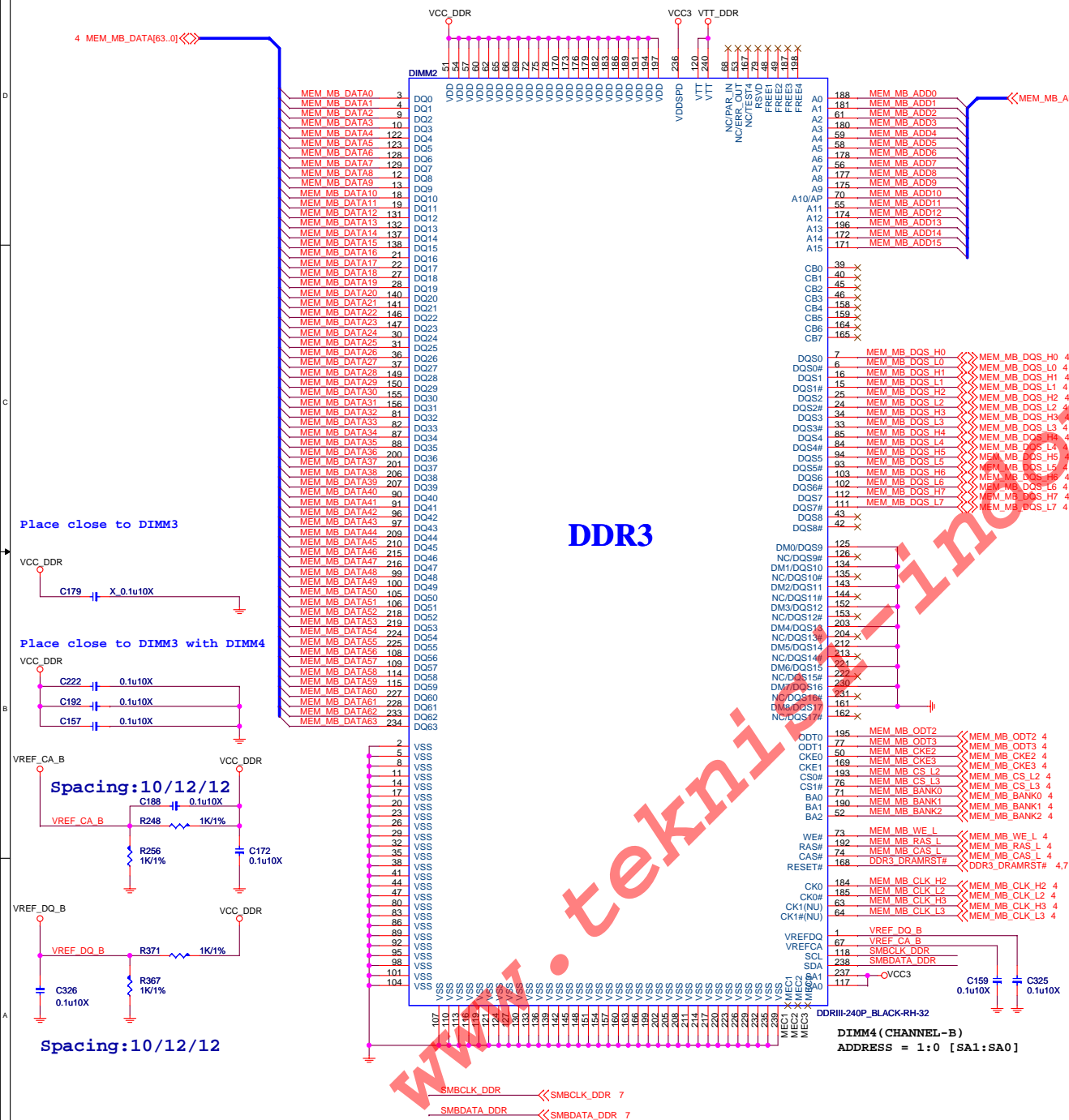


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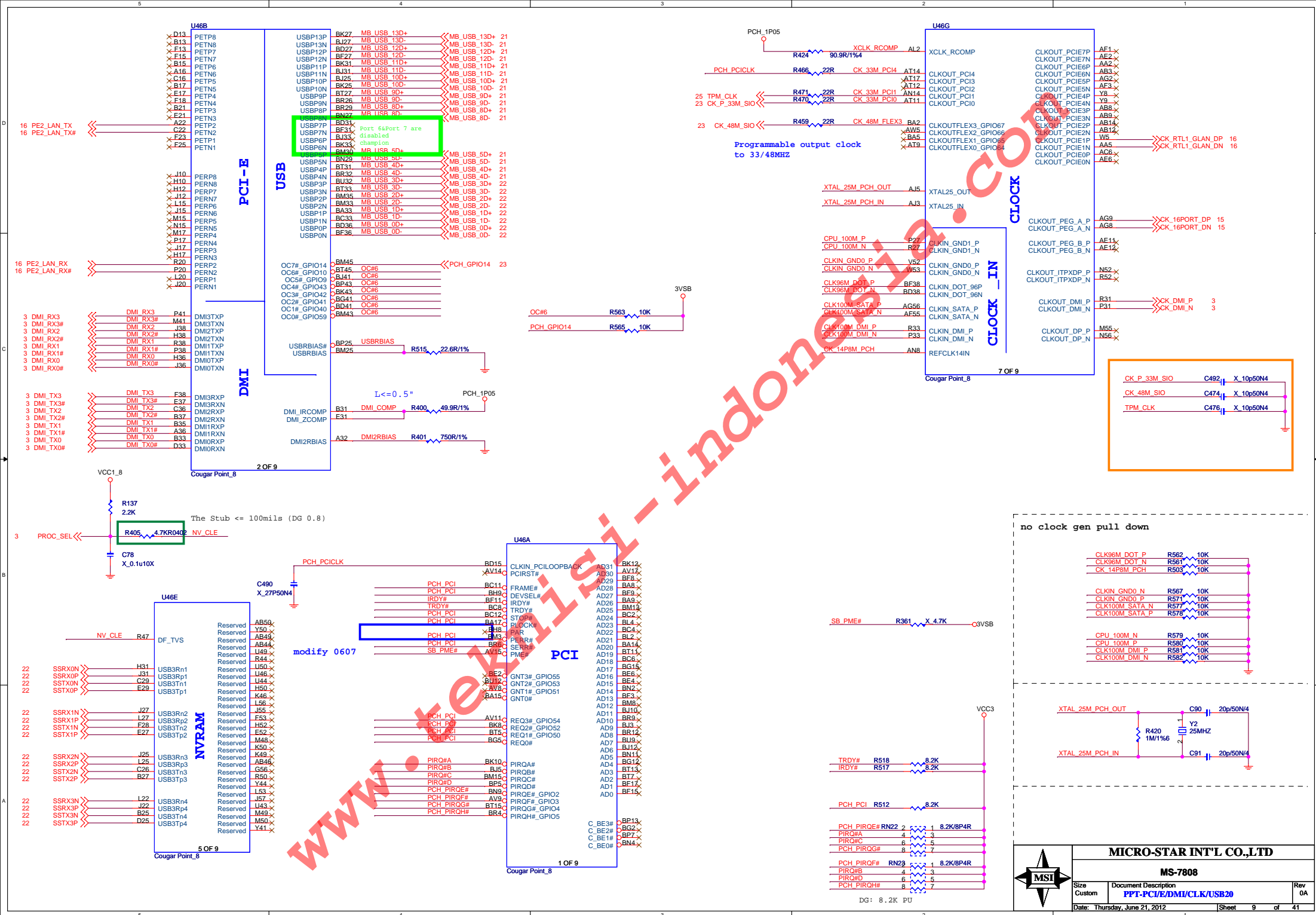
DDRIII DIMM_B0

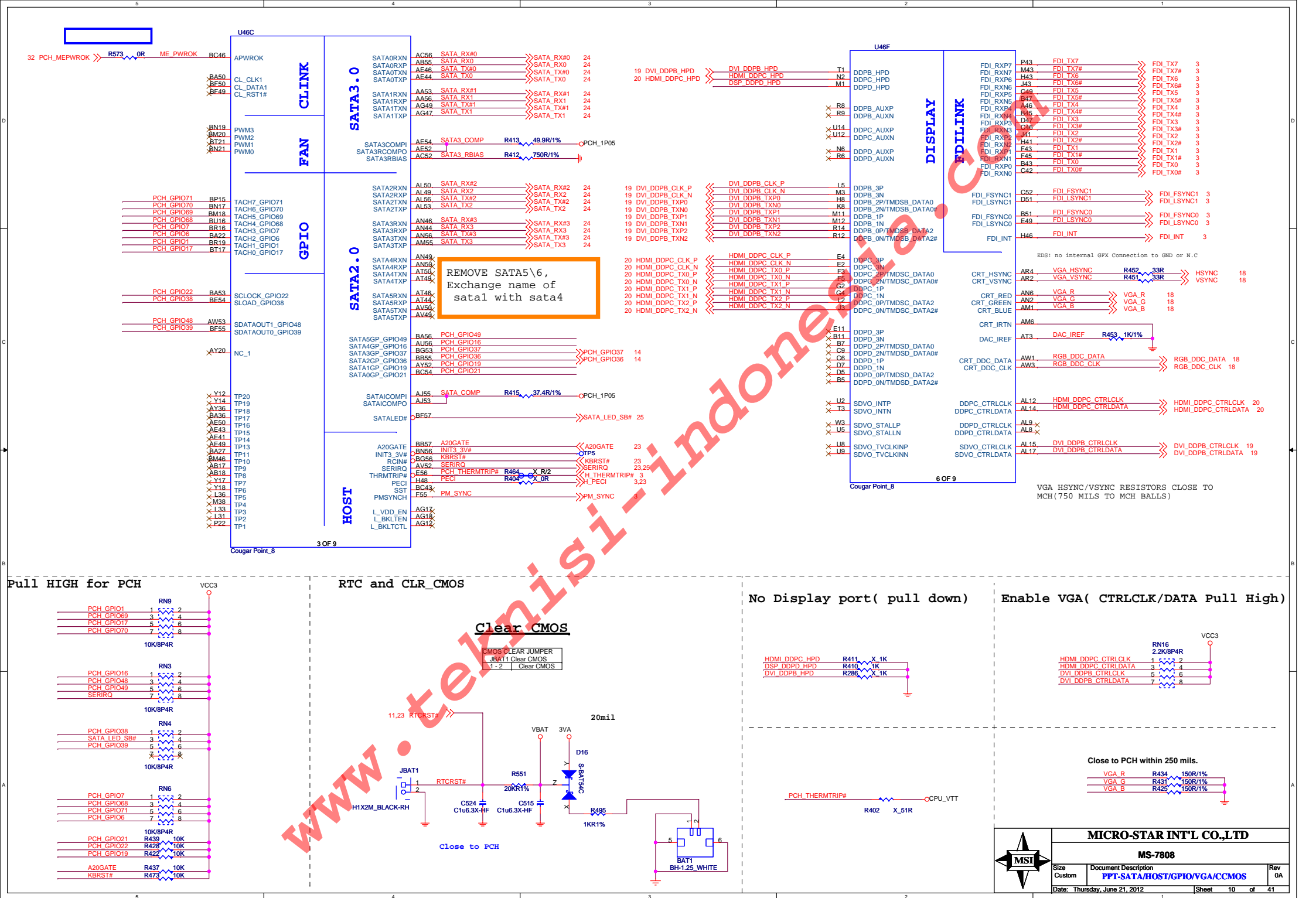


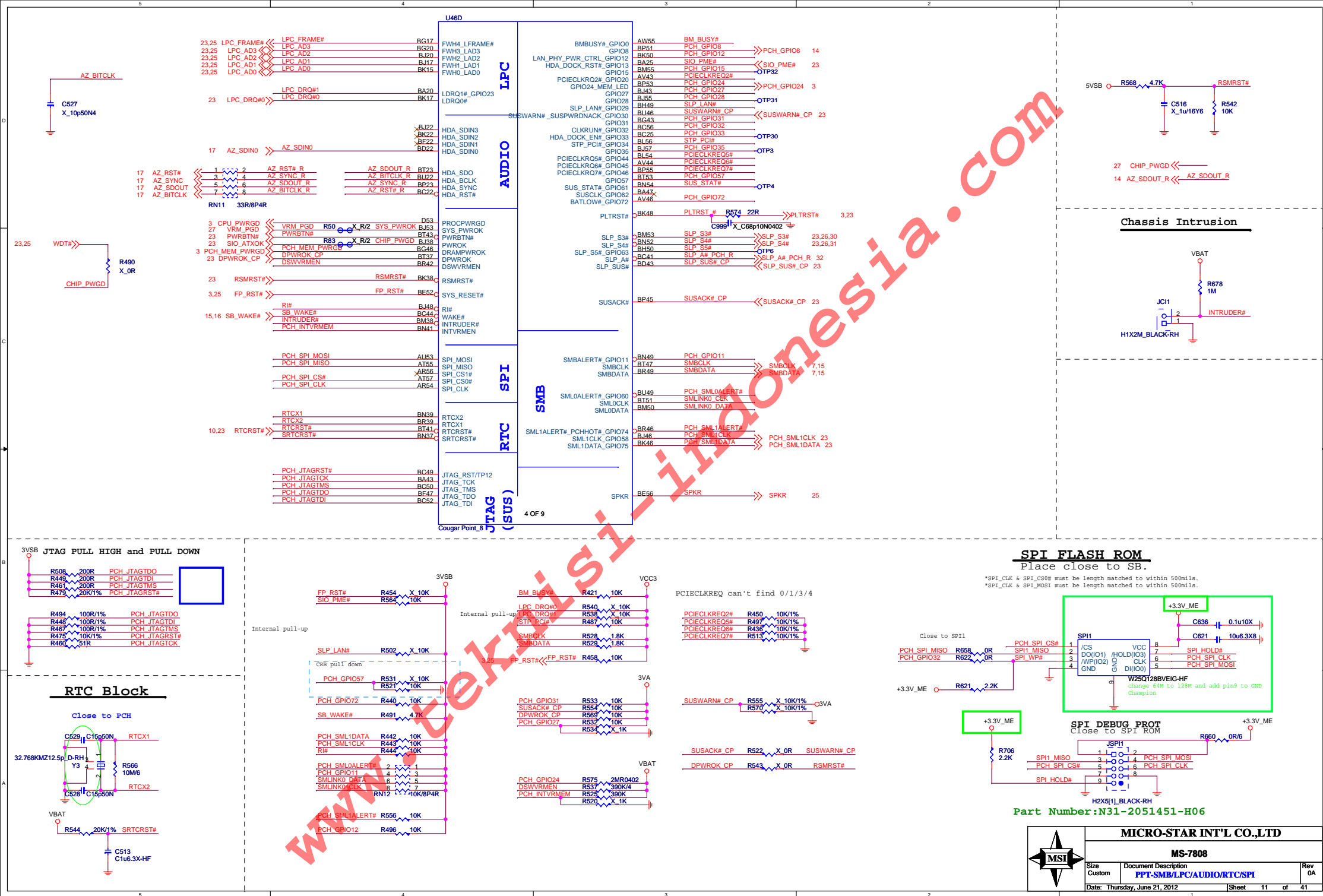
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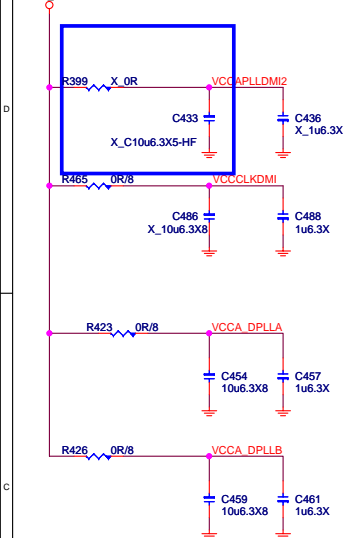
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PCH_1P05

DMI PLL FILTER

L24

X_1IU_500mA_0805

VCCAPLLEXP

C429

X_10uF6.3X

C442

X_1uF6.3X

SATA PLL FILTER

L25

X_110U_100mA_0805

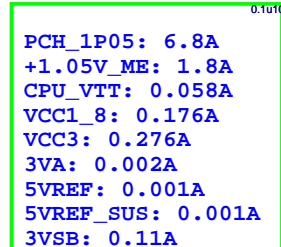
VCCAPLLSATA

C450

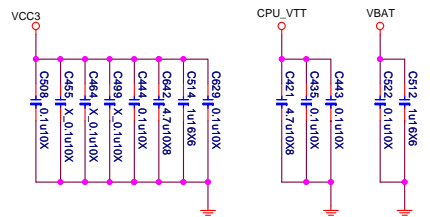
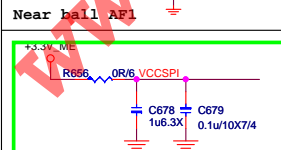
X_10uF6.3X

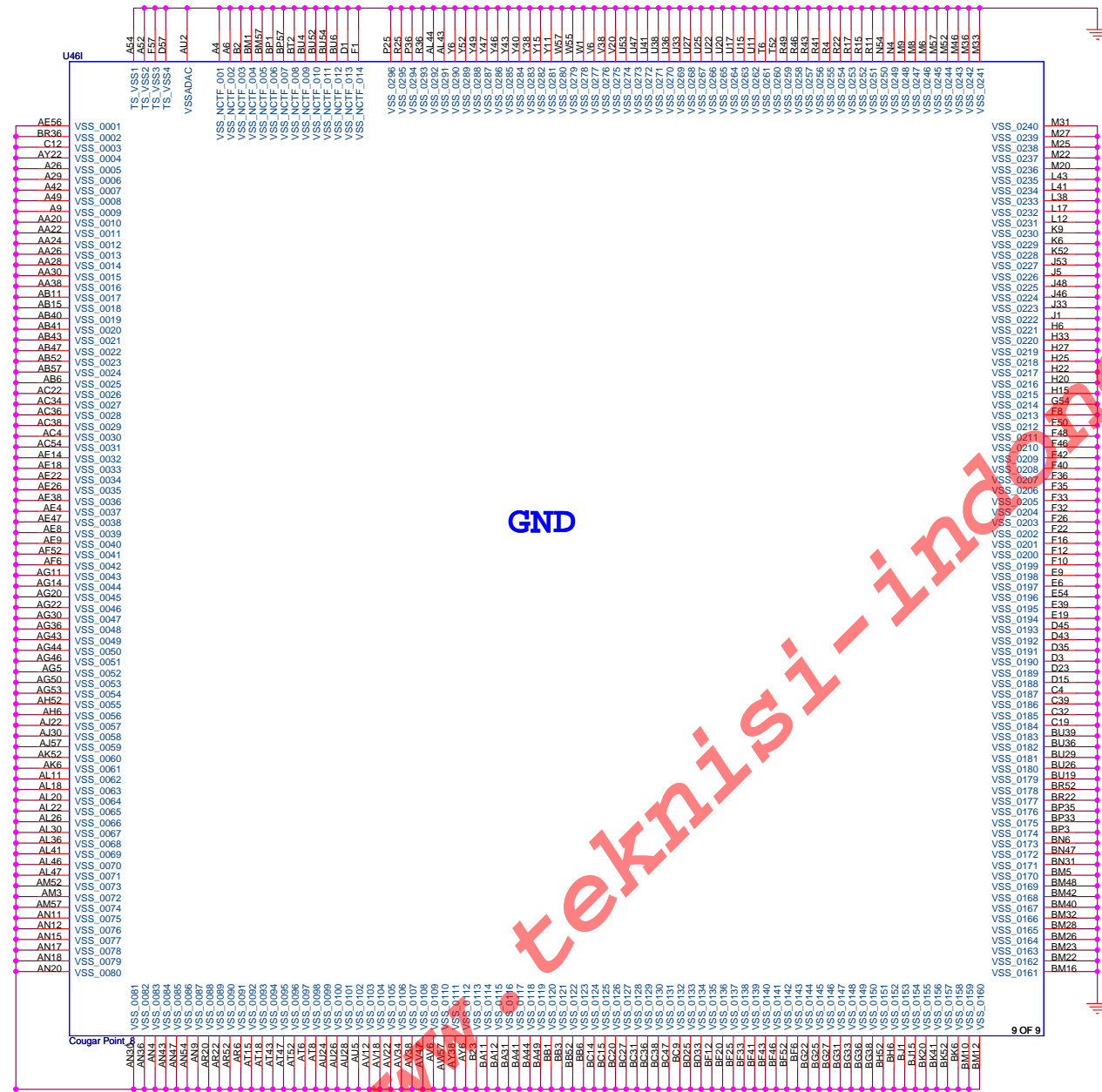
C449

X_1uF6.3X



The diagram shows a 5V reference circuit. It consists of two 2N3904 transistors, Q55 and Q57. Transistor Q55 has its base connected to VCC3 and its emitter connected to a 10R resistor, which is connected to VCC5. The collector of Q55 is connected to a 1u6.3X capacitor, which is connected to ground. Transistor Q57 has its base connected to 3VSB and its emitter connected to a 100R/1% resistor, which is connected to 5VSB. The collector of Q57 is connected to a 0.1u10X capacitor, which is connected to ground. Both capacitors are connected to a common 5VREF node.





PCH Straps



SPKR
0 : Default Mode:
1 : No Reboot Mode with TCO Disabled:



Internal pull-up
Do not pull low.



HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY
Internal weak pull down. Do not pull up.



Enable TLS:GPIO15
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.



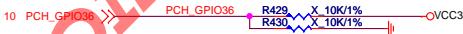
BTM
Leave floating. Do not pull low.
FCIM
Pull low with 1k Ohm to ground.
FCIM. Can be override by
Softstrap through ME.



Default
Do not pull high.
Disable ME in Manufacturing Mode
Connect to VccSusHDA with 1k Ohm pull-up
resistor through a jumper.



Internal weak pull up. Do not pull low.
On die PLL voltage regulator



Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

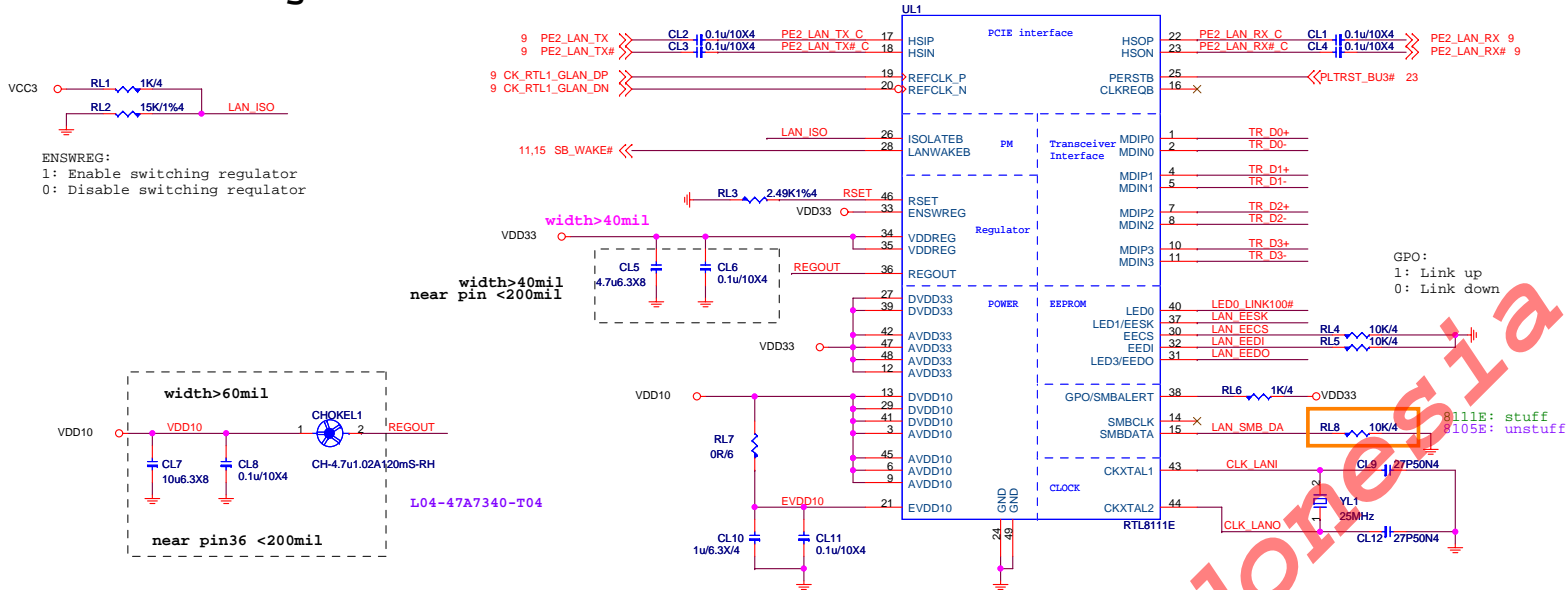


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a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.



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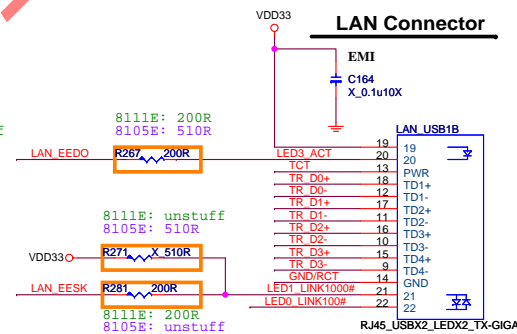
RTL8111E Giga LAN



8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

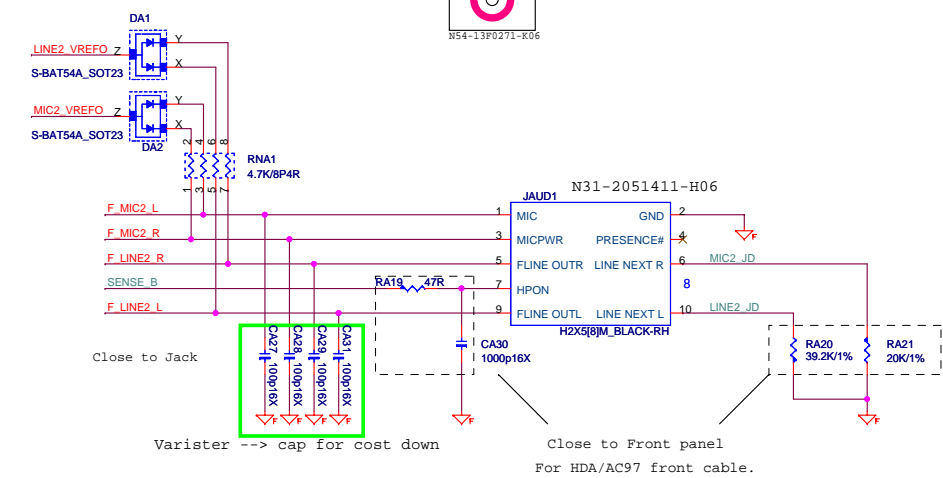
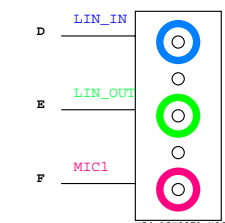
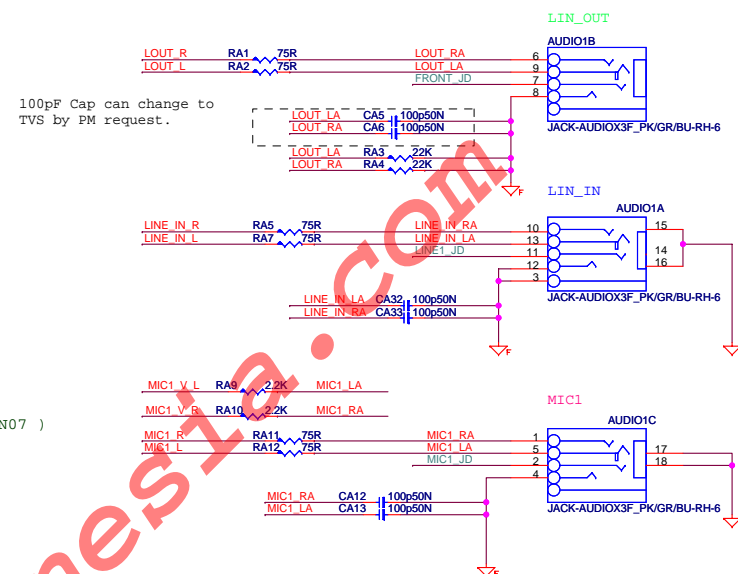
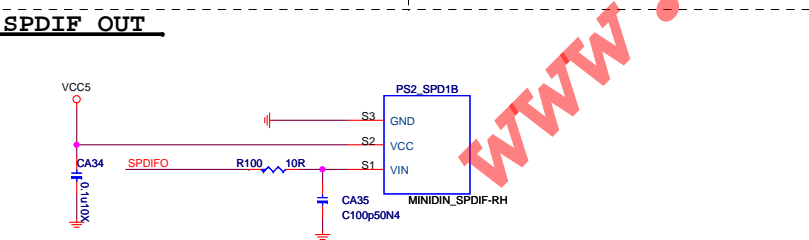
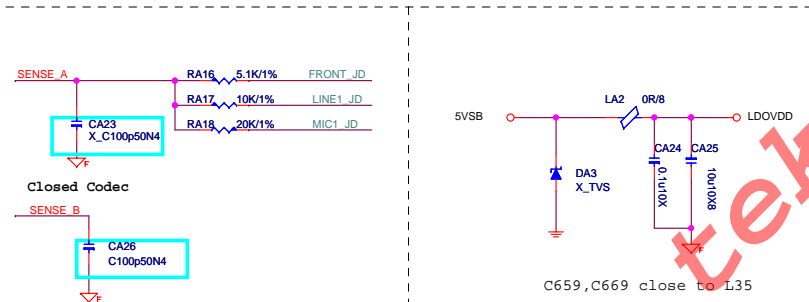
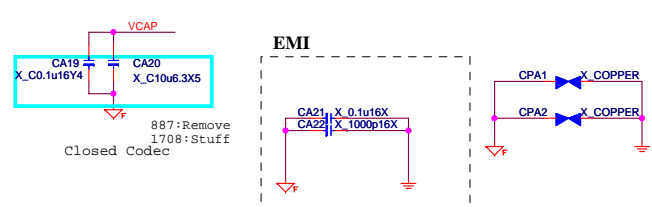
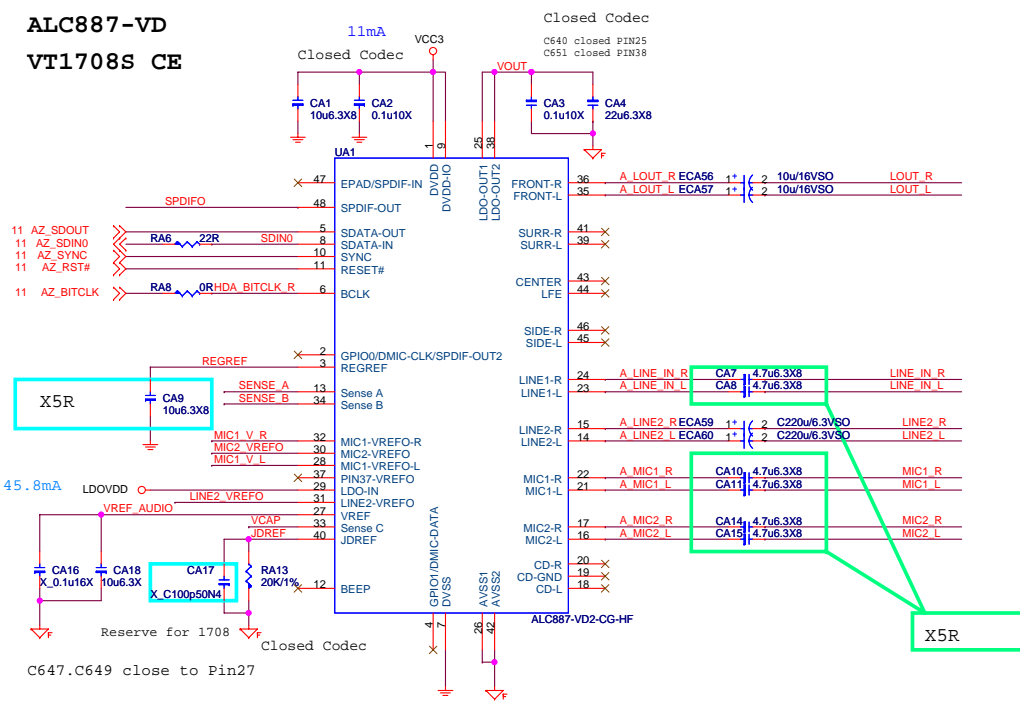
LAN Connector



only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	1000 Orange
100 Green	100 Green
10 None	10 None
19	19
20	20
21	21
22	22

ALC887-VD
VT1708S CE



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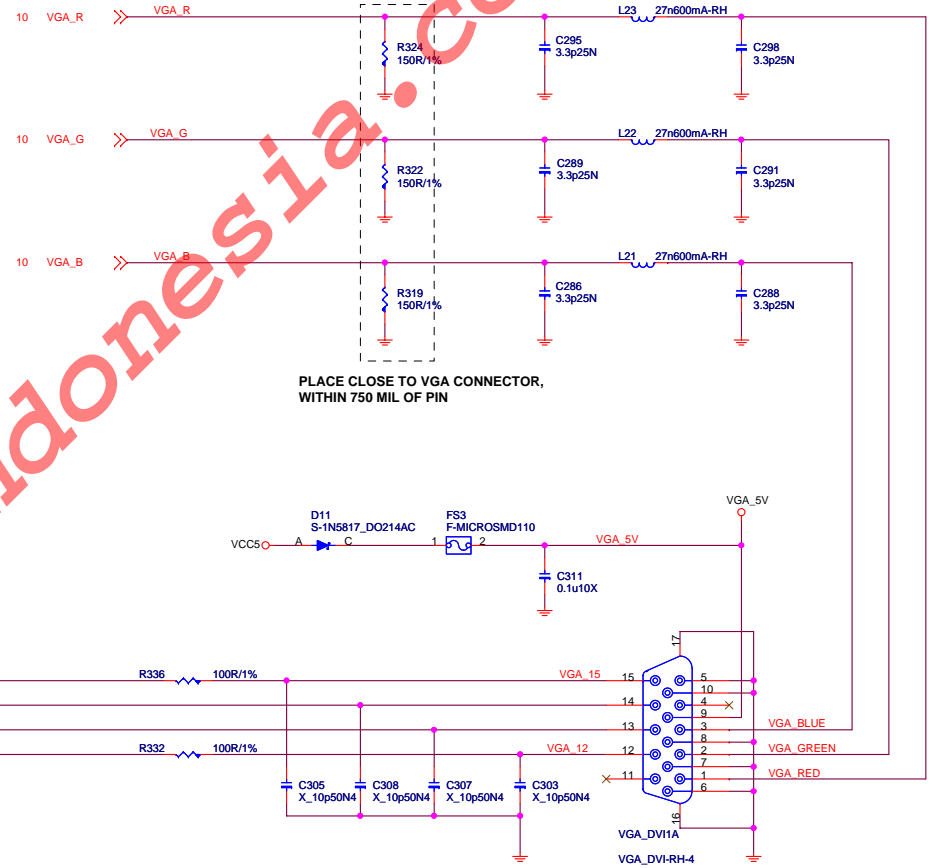
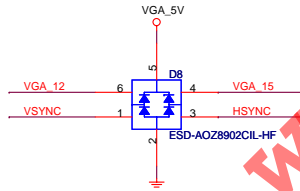
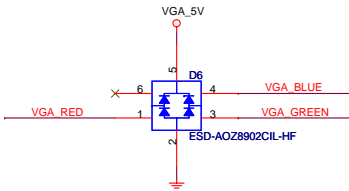
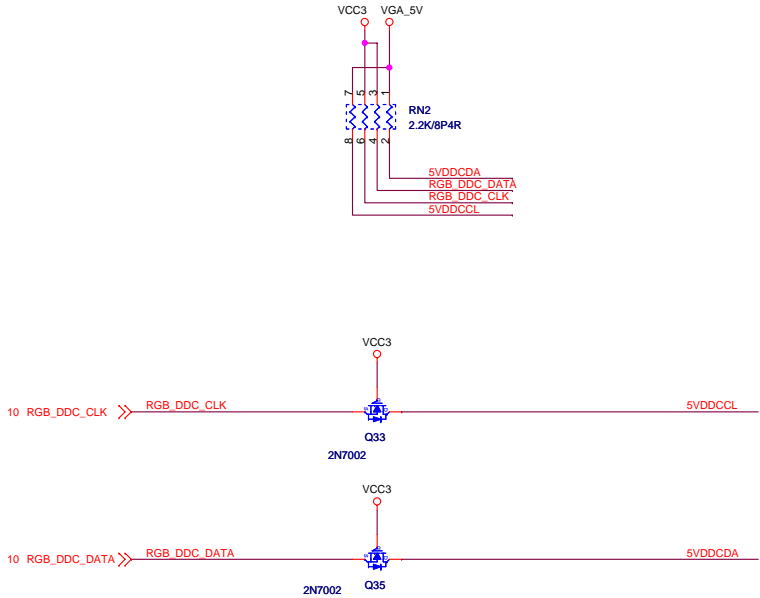
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D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Levelshift

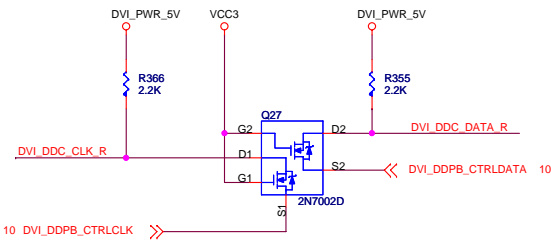


PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

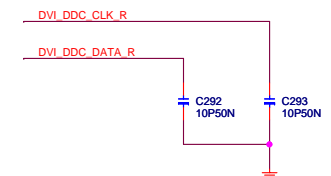
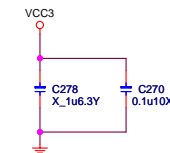
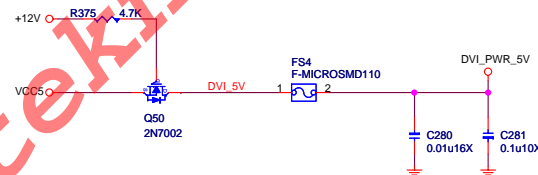
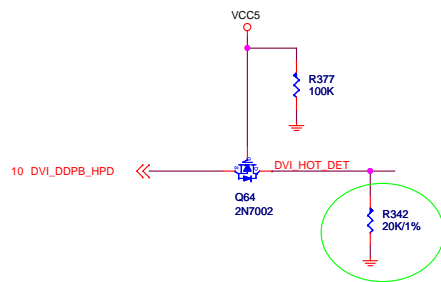
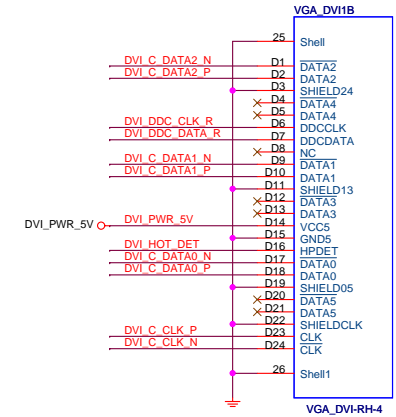
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 10 DVI_DDPB_CLK_P C336 0.1u10X DVI_C_CLK_P R524 680R DVI_DATA_CLK_DP
 10 DVI_DDPB_TXN0 C362 0.1u10X DVI_C_DATA0_N R493 680R DVI_DATA0_DN
 10 DVI_DDPB_TXP0 C361 0.1u10X DVI_C_DATA0_P R507 680R DVI_DATA0_DP
 10 DVI_DDPB_TXN1 C336 0.1u10X DVI_C_DATA1_N R519 680R DVI_DATA1_DN
 10 DVI_DDPB_TXP1 C339 0.1u10X DVI_C_DATA1_P R523 680R DVI_DATA1_DP
 10 DVI_DDPB_TXN2 C364 0.1u10X DVI_C_DATA2_N R526 680R DVI_DATA2_DN
 10 DVI_DDPB_TXP2 C363 0.1u10X DVI_C_DATA2_P R514 680R DVI_DATA2_DP

C353 3.9950N
 C351 3.9950N
 C340 3.9950N
 C342 3.9950N
 C343 3.9950N
 C344 3.9950N
 C345 3.9950N
 C346 3.9950N
 C347 3.9950N
 C348 3.9950N
 C349 3.9950N

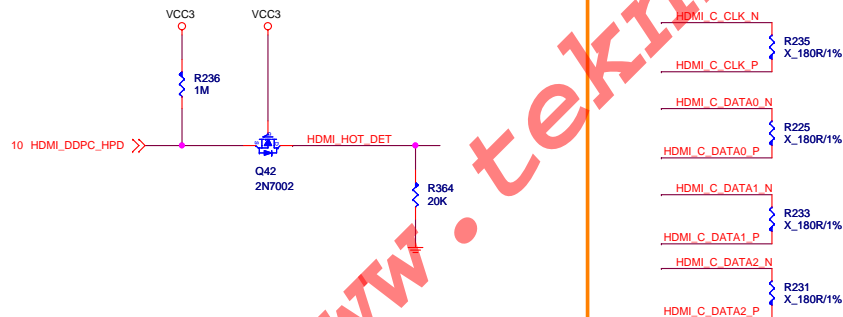
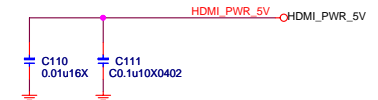
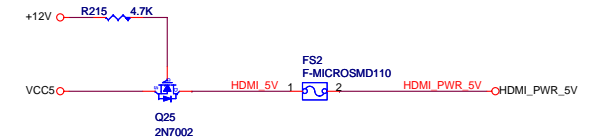
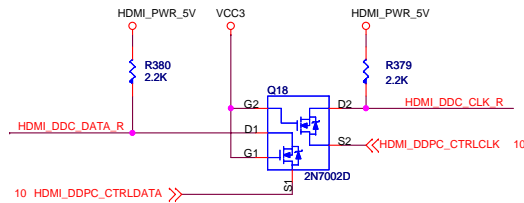


For EMI

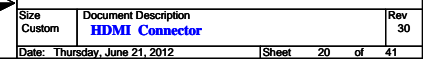
DVI_C_DATA0_N R871 243R/1%
 DVI_C_DATA0_P R871 243R/1%
 DVI_C_DATA1_N R874 243R/1%
 DVI_C_DATA1_P R874 243R/1%
 DVI_C_CLK_N R873 243R/1%
 DVI_C_CLK_P R873 243R/1%
 DVI_C_DATA2_N R872 243R/1%
 DVI_C_DATA2_P R872 243R/1%



10	HDMI_DDPCC_CLK_P	1C140	0.1u10X	HDMI_C_CLK_P	R545	680R	HDMI_D
10	HDMI_DDPCC_CLK_N	1C142	0.1u10X	HDMI_C_CLK_N	R558	680R	HDMI_D
10	HDMI_DDPCC_TX2_P	1C142	0.1u10X	HDMI_C_DATA2_P	R527	680R	HDMI_D
10	HDMI_DDPCC_TX2_N	1C132	0.1u10X	HDMI_C_DATA2_N	R549	680R	HDMI_D
10	HDMI_DDPCC_TX1_P	1C136	0.1u10X	HDMI_C_DATA1_P	R550	680R	HDMI_D
10	HDMI_DDPCC_TX1_N	1C136	0.1u10X	HDMI_C_DATA1_N	R548	680R	HDMI_D
10	HDMI_DDPCC_TX0_P	1C124	0.1u10X	HDMI_C_DATA0_P	R553	680R	HDMI_D
10	HDMI_DDPCC_TX0_N	1C121	0.1u10X	HDMI_C_DATA0_N	R548	680R	HDMI_D



HDMI DDC CLK R	C572	X 0.1u16X
HDMI DDC DATA R	C571	X 0.1u16X
HDMI HOT DET	C570	X 0.1u16X

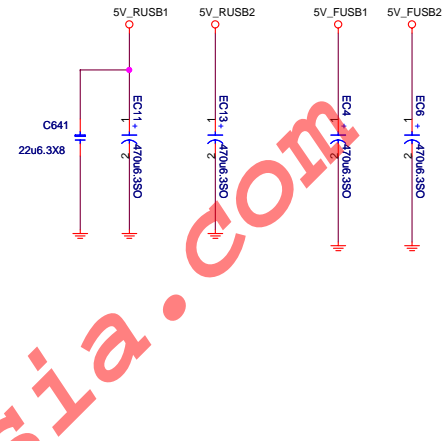
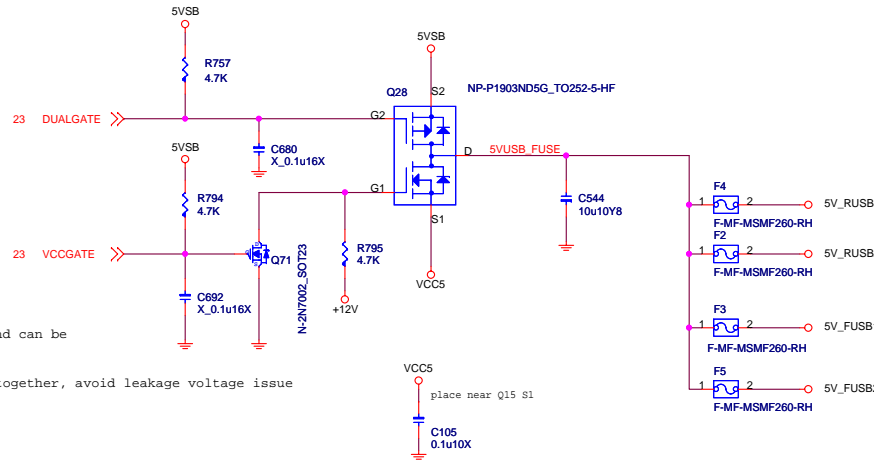


USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	1	1	1
S0P5_Gate#	1	1	0

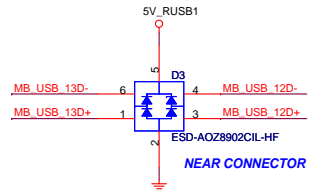
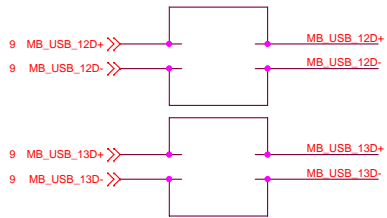
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	0	1	1
S0P5_Gate#	1	1	0

*In S5# (S3P5_Gate # pin status is Tri-state, and can be programmed Low level.

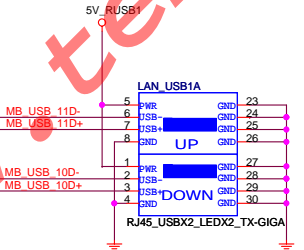
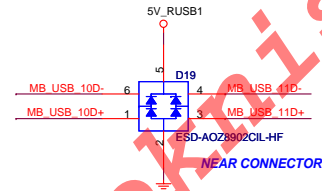
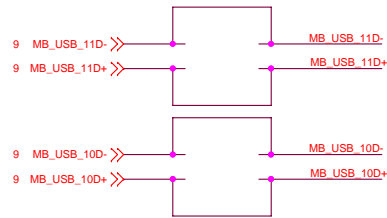
*S3P5_Gate# and S0P5_Gate# can't setting to low together, avoid leakage voltage issue



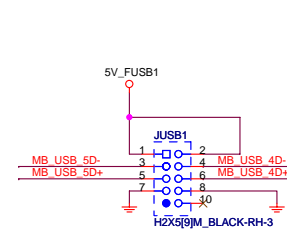
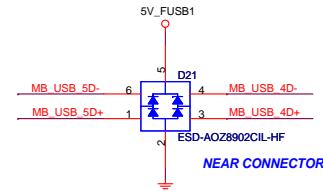
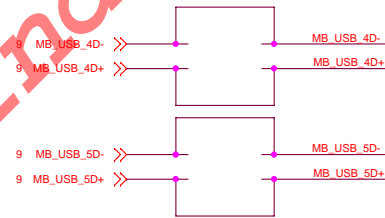
REAR USB PORT 12,13



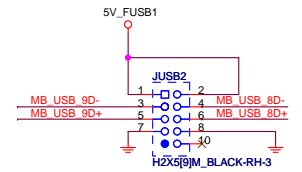
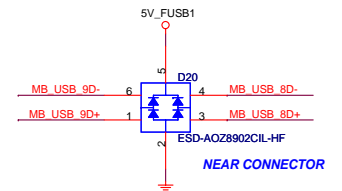
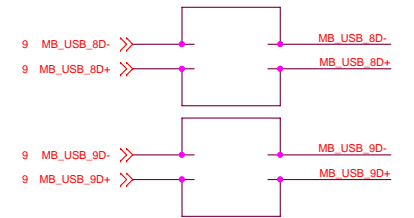
FRONT USB PORT 10,11(With LAN)

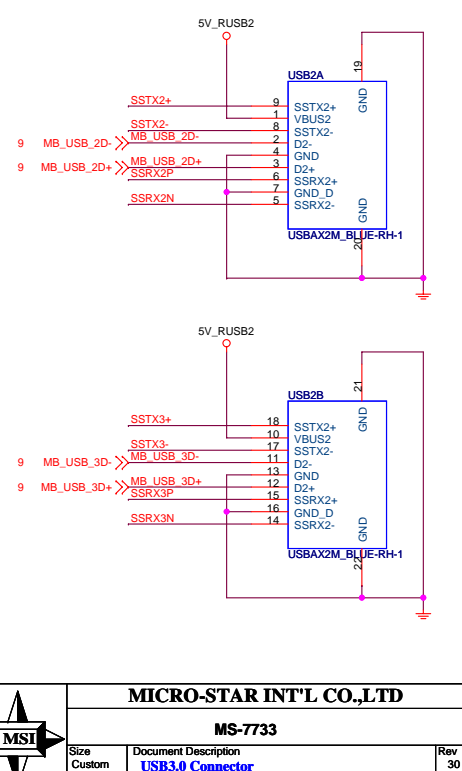
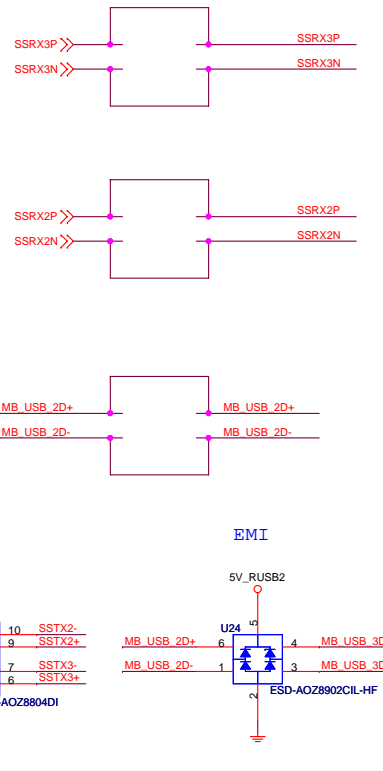
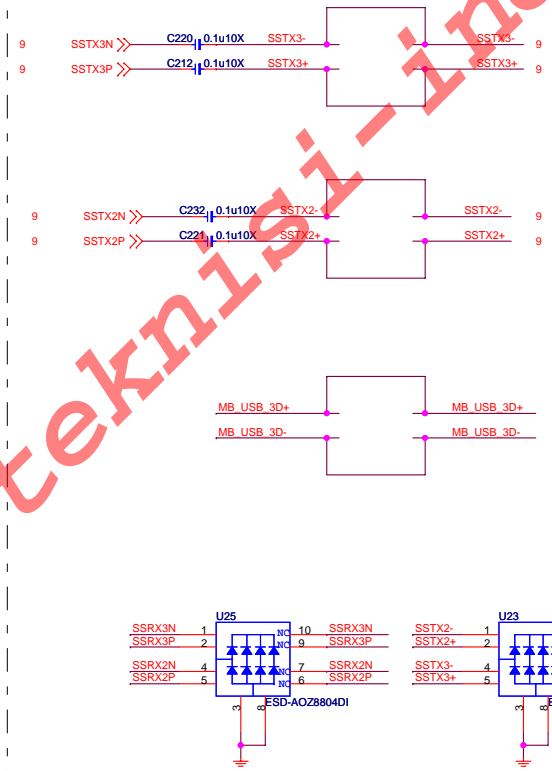
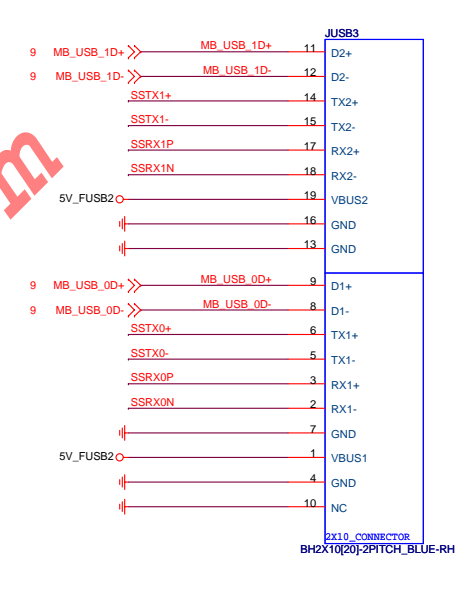
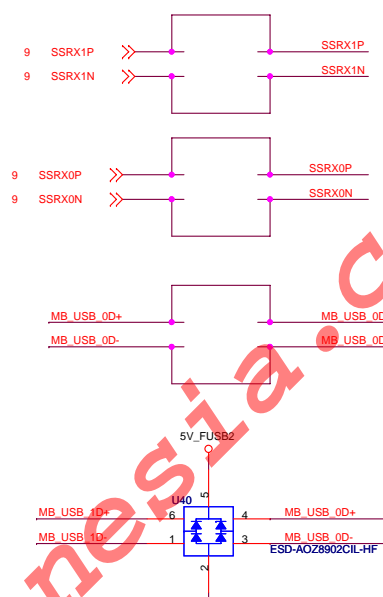
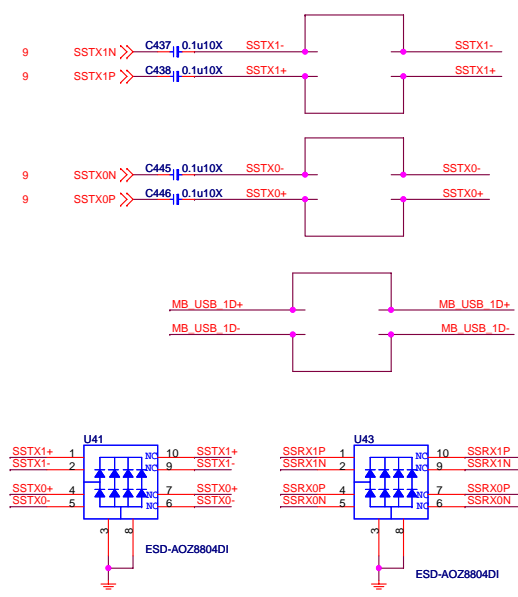


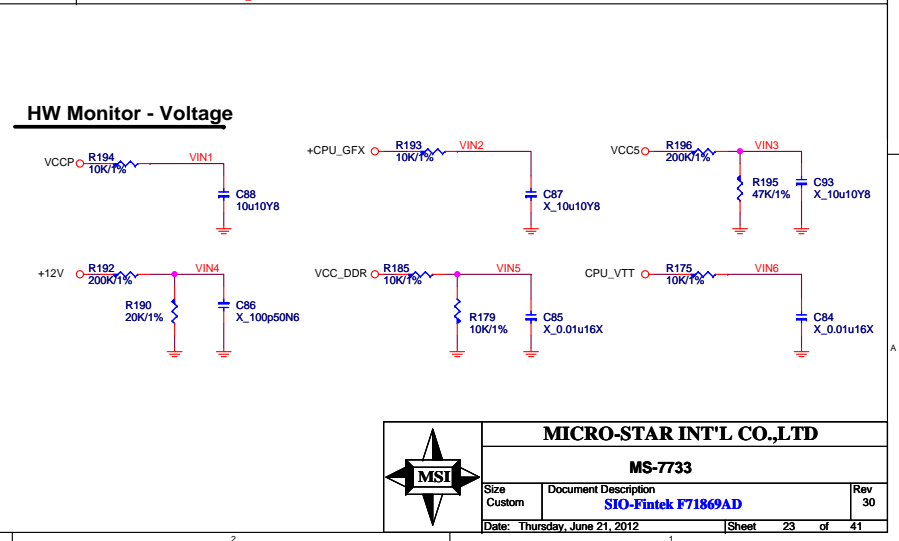
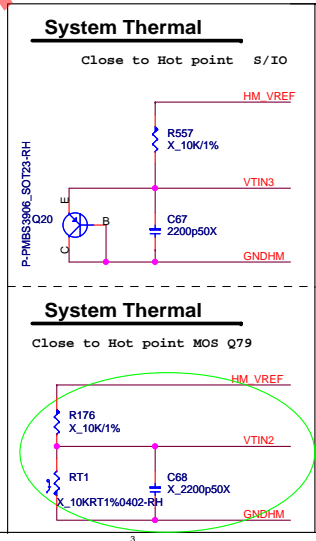
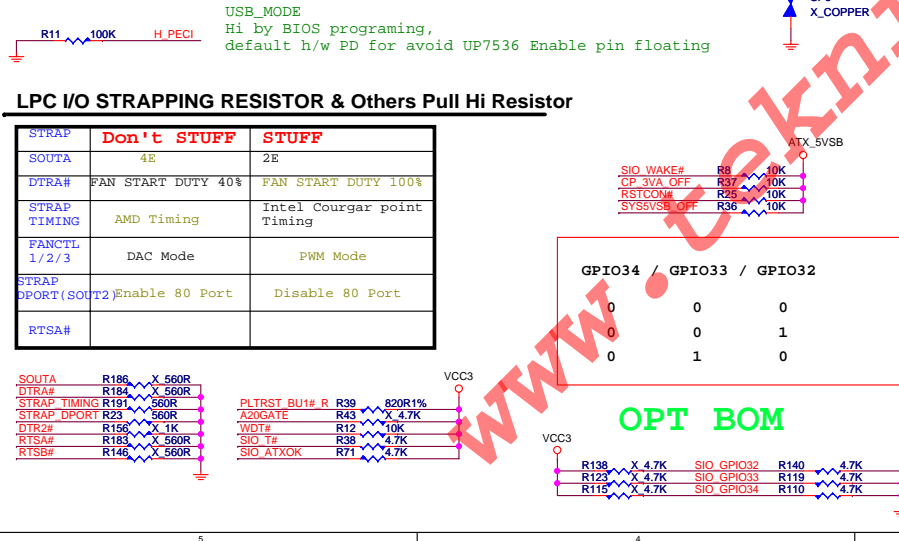
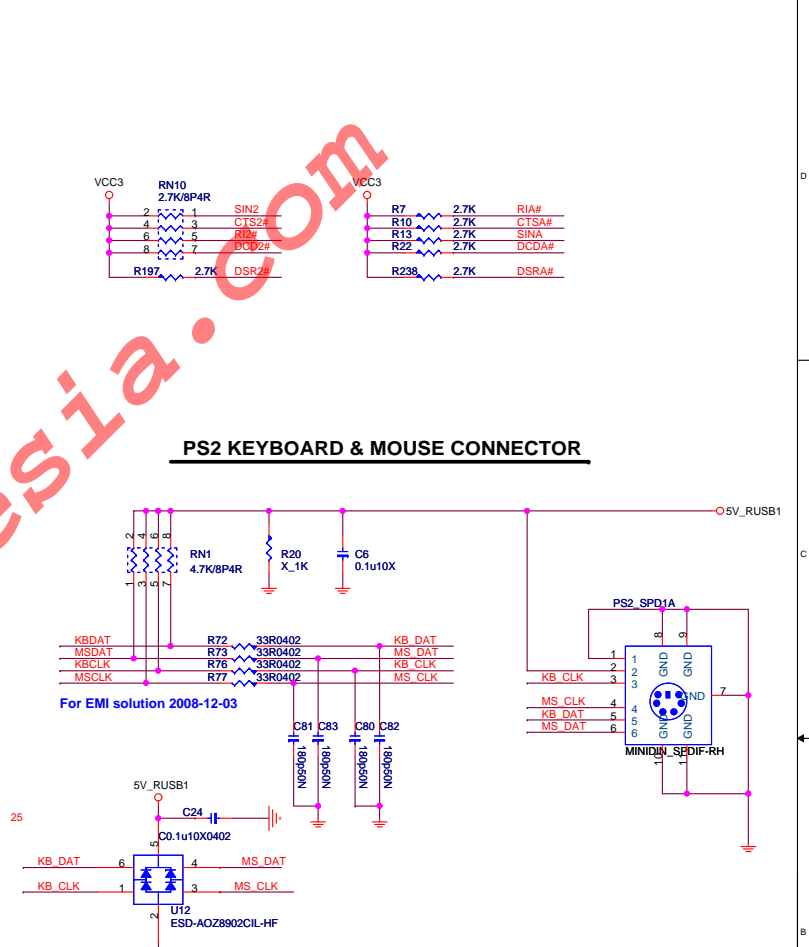
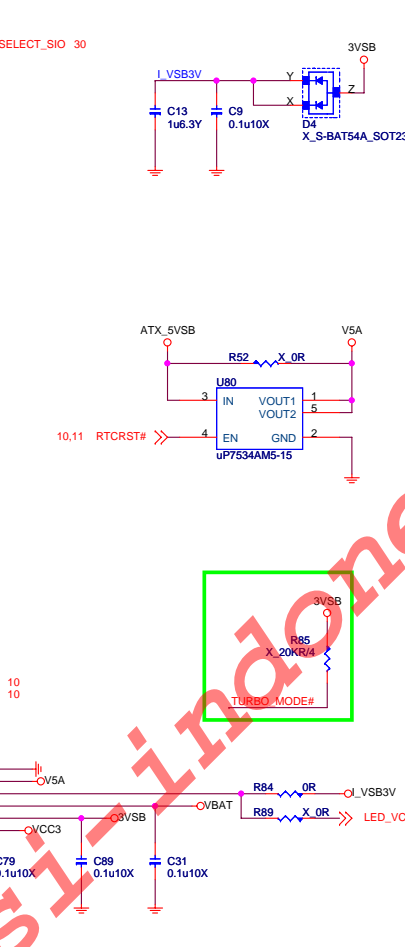
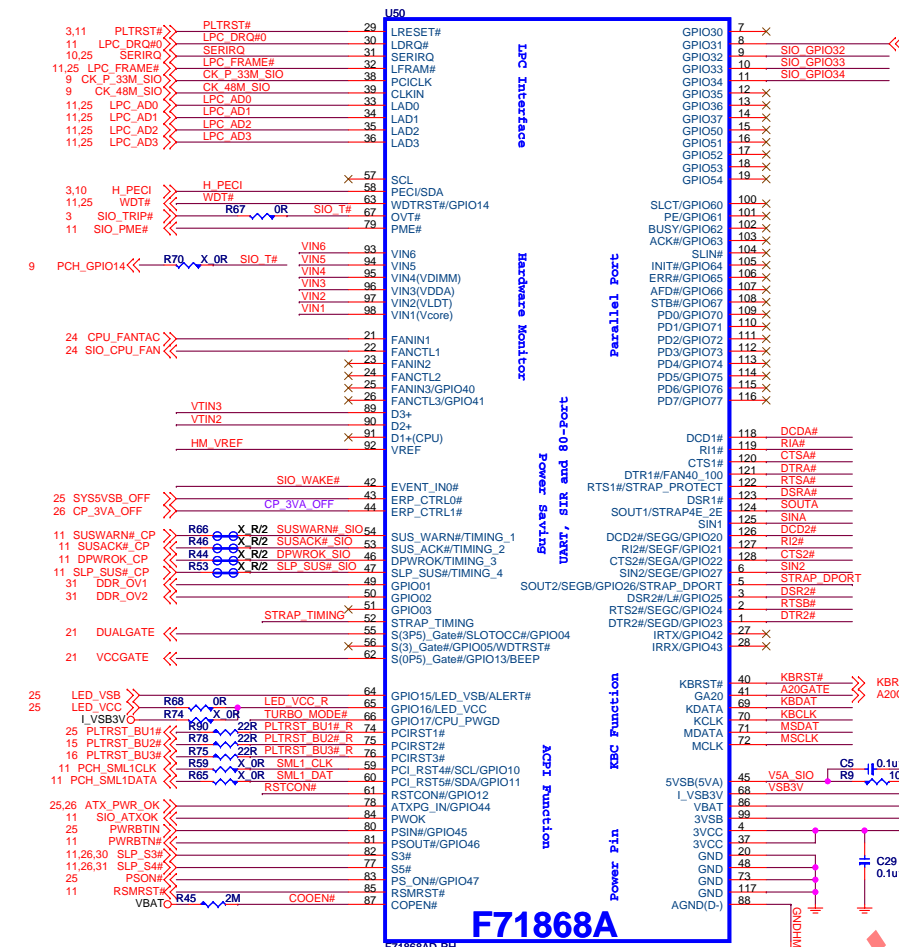
FRONT USB PORT 4,5



FRONT USB PORT 8,9

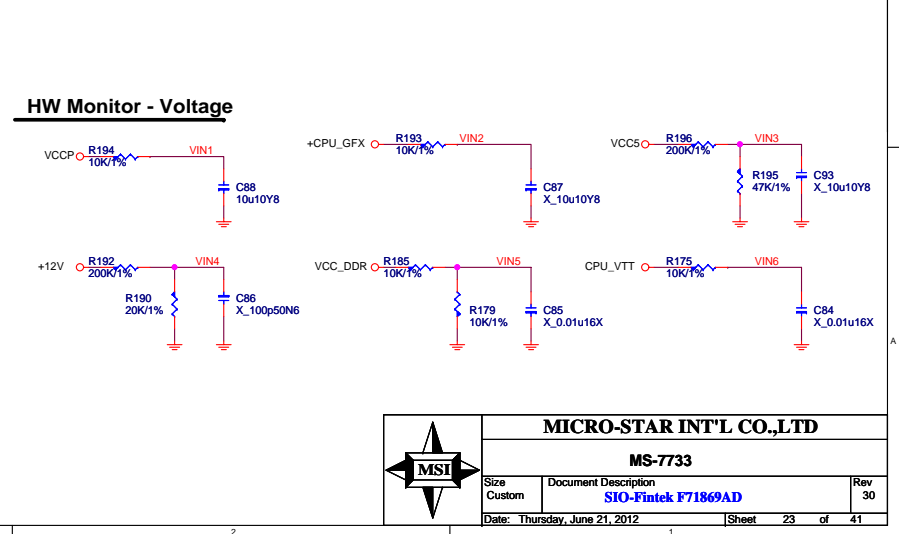
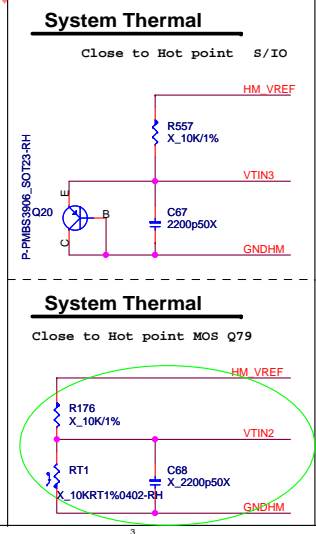
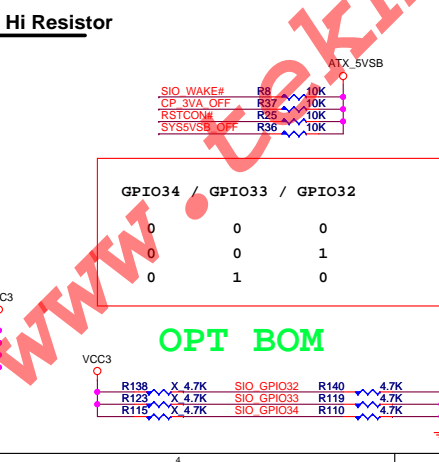
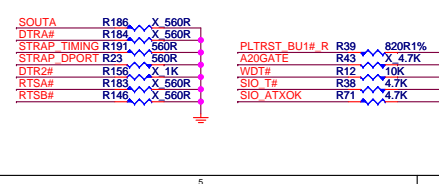






LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courgar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT(SOUT2)	Enable 80 Port	Disable 80 Port
RTSA#		



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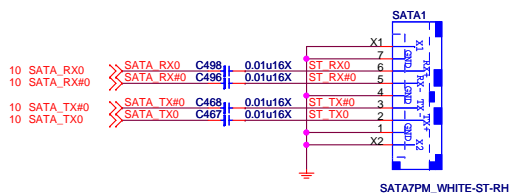
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Custom	SIO-Fintek F71869AD	30

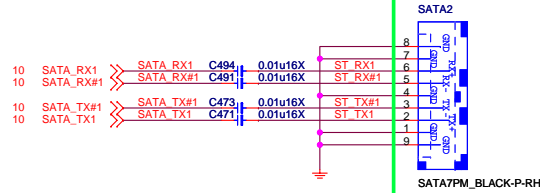
Date: Thursday, June 21, 2012

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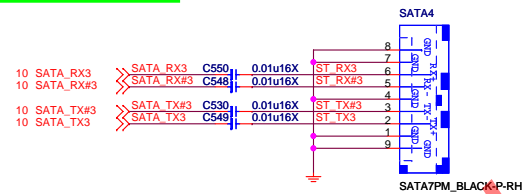
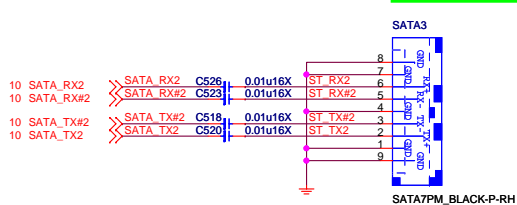
3.0 white



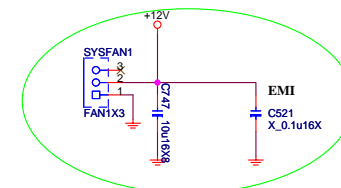
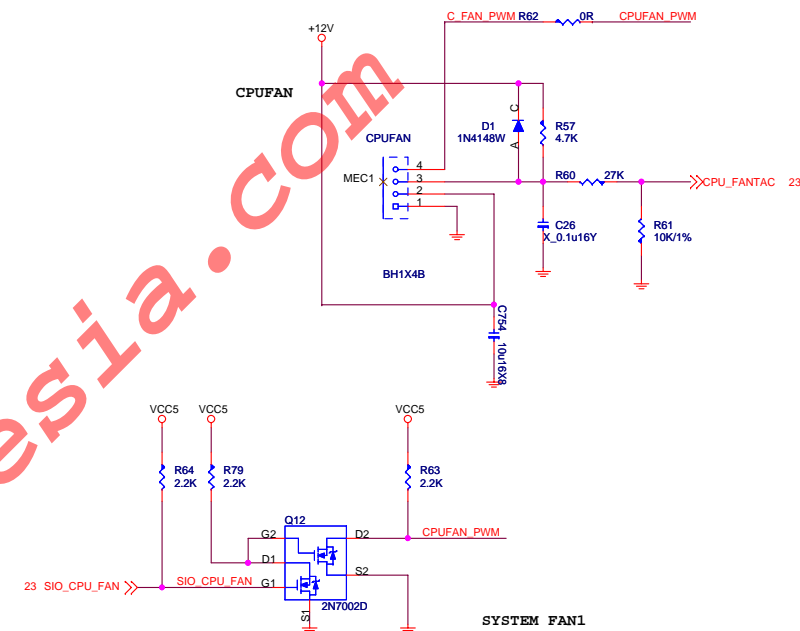
2.0 Black



2.0 Black



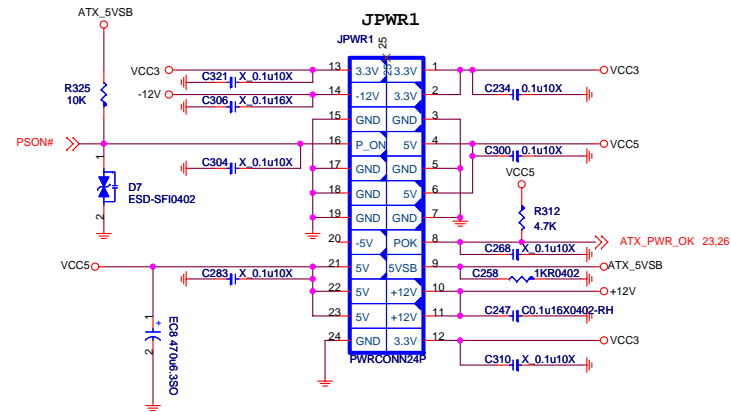
FAN-COUNTROL CIRCUIT



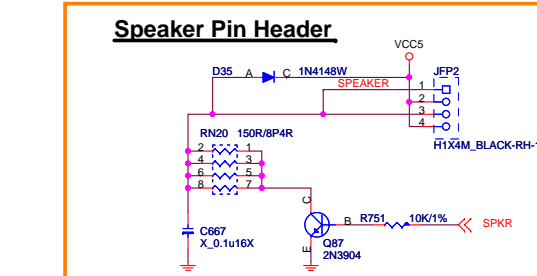
MS-7733

Size Custom	Document Description FAN Control	Rev 30
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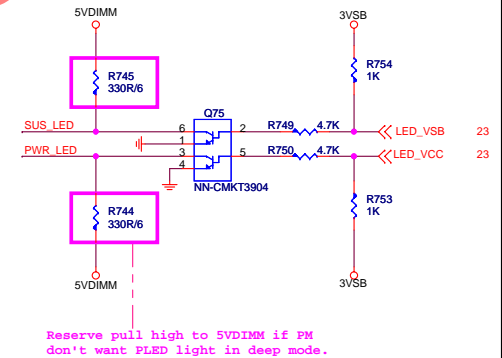
ATX POWER CONNECTOR



Speaker Pin Header

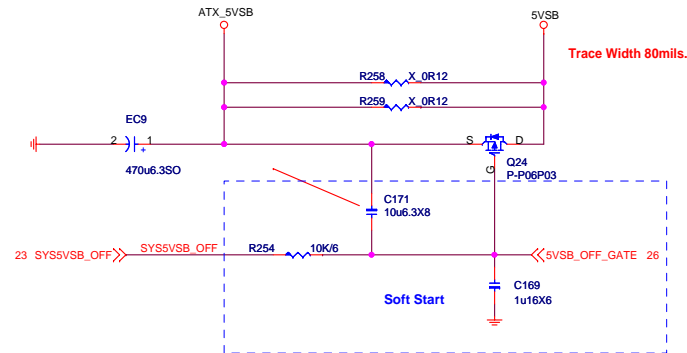


LED (for Fintek 71869)

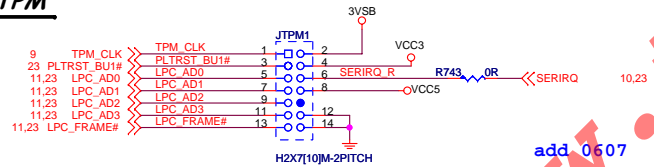


5VSB Power Switch

Tune 5VSB inrush current to 2A from 4A



TPM



5VDIMM FOR DDR

VCC5

23.25 ATX_PWR_OK

11.23.30 SLP_S3#

11.23.31 SLP_S4#

31 SLP_S5_LCH#

R81 510R

R80 10K/1%

R103 0R

R111 X_0R

U5

S3#

S5#

MODE

uP7501

5VSB_DRV

5VSB_DRV

5VDIMM_5VSB

R99 10R

C48 0.1u10X

5VSBDRV1

5VDRV1

R86 1K/1%6

C35 22n16X

+12V

G2

G1

S2

S1

Q15

D

NP-P200ND5G

VCC5

C103 0.1u10X

C46 18n16X

C104 0.1u10X

place near Q15 S1

7501 Mode

H:Support S0/S3/S5

L:Support S0/S3

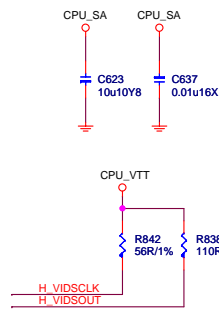
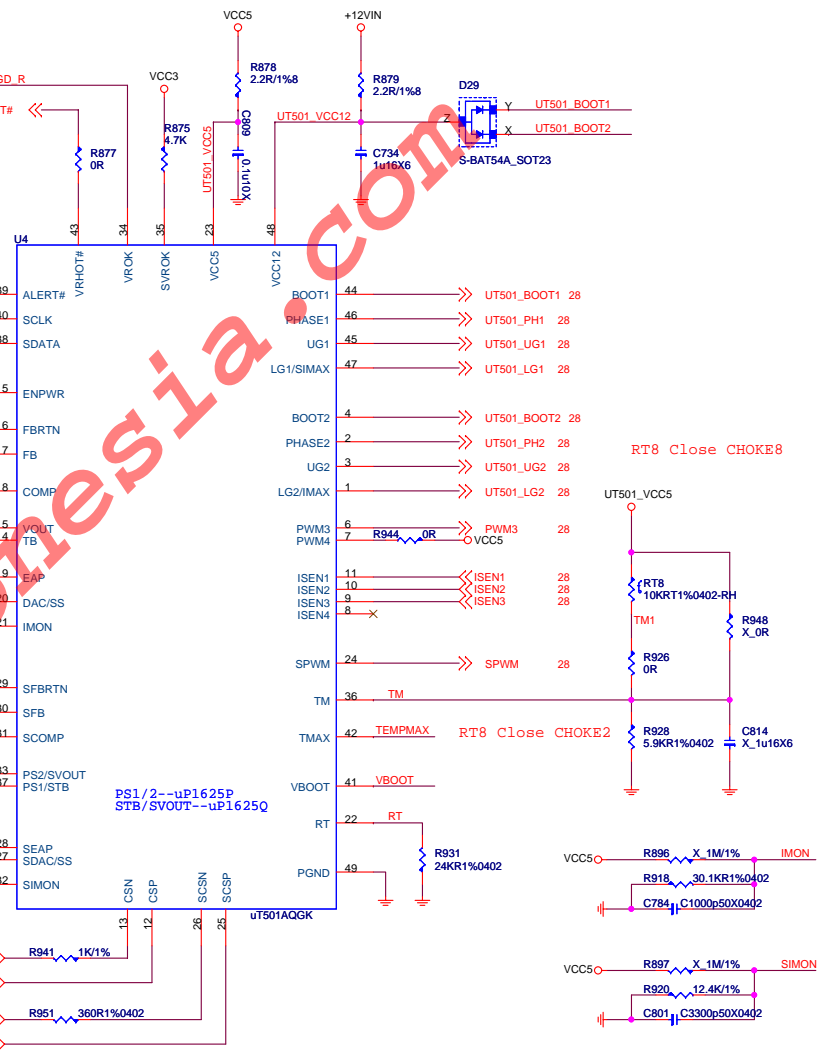
The circuit diagram shows a power MOSFET driver stage. A green box highlights the input buffer and gate drive network. It includes a 5VSB supply connected to a 47kΩ resistor (R441) and a 2N7002 MOSFET (Q53). The 2N7002's gate is driven by a GATE signal through a 10nF capacitor (C470). The drain of Q53 is connected to the EN pin of a U47 OP0104SSW8_PSOP8-HF op-amp. The op-amp's non-inverting input (VIN) is also connected to the 5VSB supply. The op-amp's output (VOUT) drives the gate of an N-NTMFS4841 MOSFET (Q24) through a 10kΩ resistor (R509). The MOSFET's source is grounded, and its drain is connected to a 3VSB supply through a 3.3kΩ resistor (R499). A 100nF capacitor (C477) is connected between the 3VSB supply and ground. A 10μF capacitor (C478) is connected between the 3VSB supply and the MOSFET's drain. The MOSFET's gate is also connected to a 5VDRV1 supply through a 200kΩ resistor (R510).



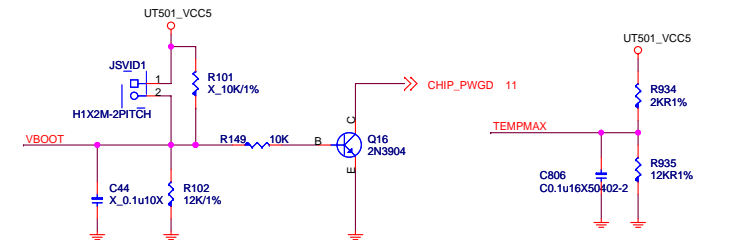
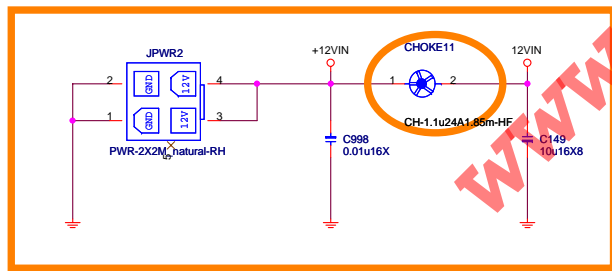
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Size Custom	Document Description ACPI controller UPI	Rev 30
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The schematic shows the VRM_PGD pin connected to a voltage divider network. CPU_VTT is connected to R29 (1K) and R28 (4.7K). 3VSB is connected to R4 (10K/1%). VCC3 is connected to R6 (4.7K) and R5 (100K). A capacitor C10 (X_0.1u/25V4) is connected to the CPU_VTT line. The network is connected to the gate of MOSFET Q1 (NN-CMKT3904). The drain of Q1 is connected to the VRM_PGD pin. The source of Q1 is connected to ground. The pin is also connected to a CRB component (Q49, X_2N7002) via a signal labeled 30 SLP_S3_CTRL#.

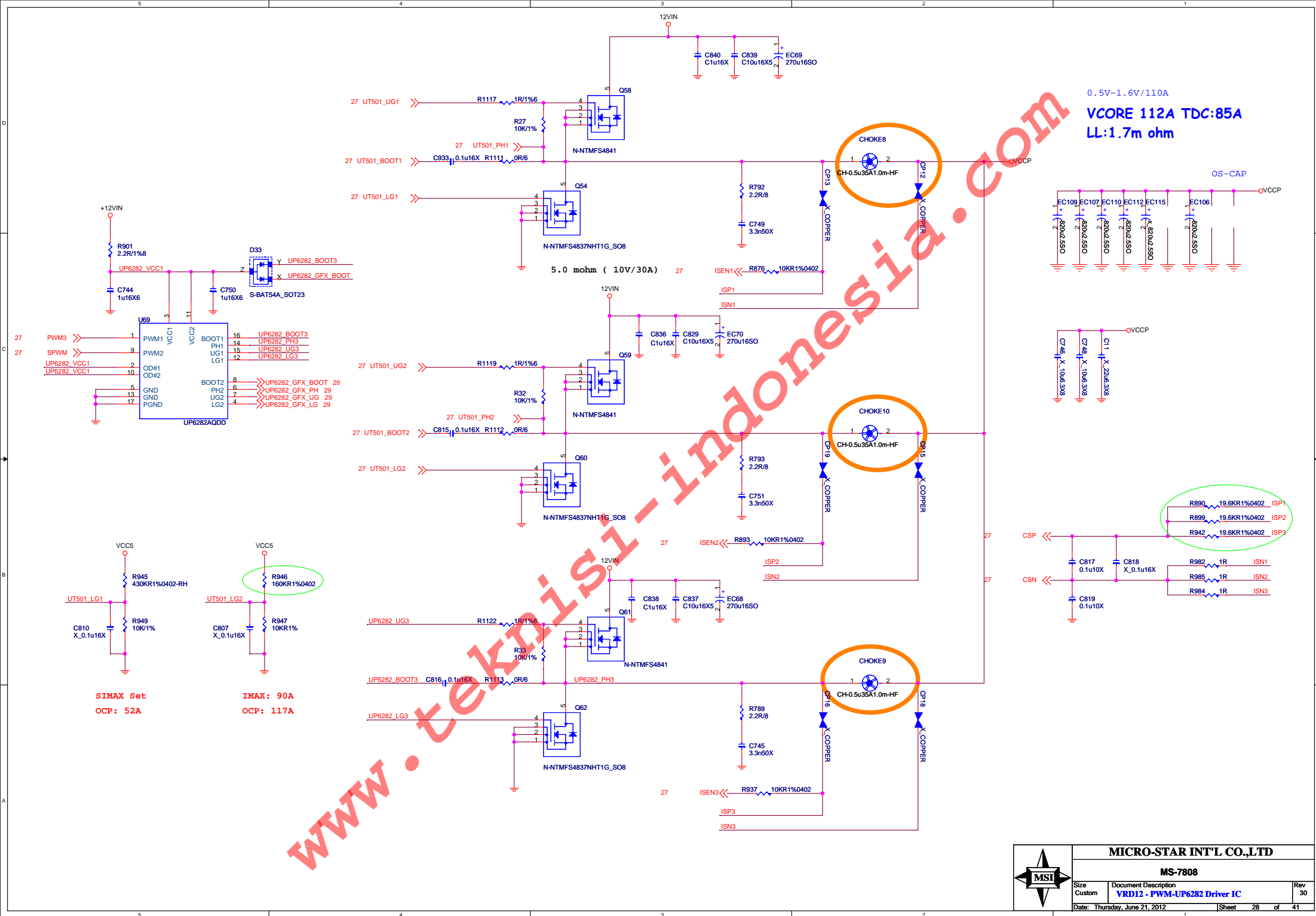
[illegible]

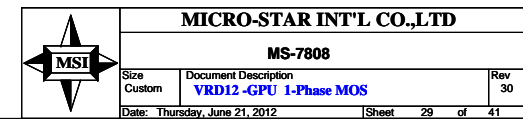
0x20: RH=10K, RL=OPEN						
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



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CPU_VTT:1.05/1.00 MAX 24.3A

CPU VTT 8.5A SA Core =8.8A PCH Core =7A

8.5A FOR CPU

Iripple=1.92(vtt)+1.88(sa)

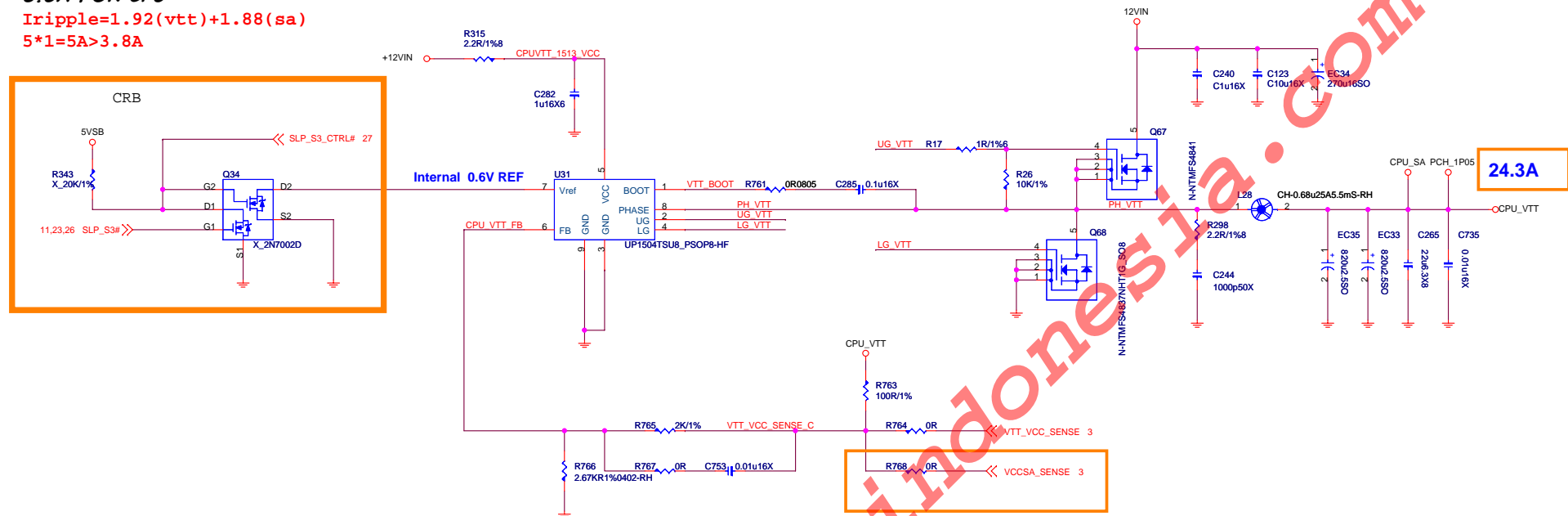
5*1=5A>3.8A

Iripple=6.2

4.7*1A<6.2A share with VCCP

Acture measure cpu_vtt max 10A

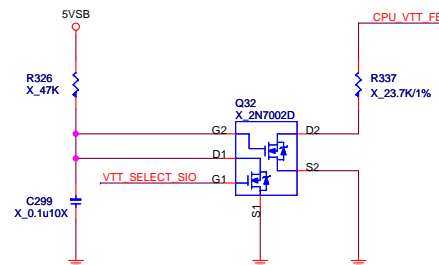
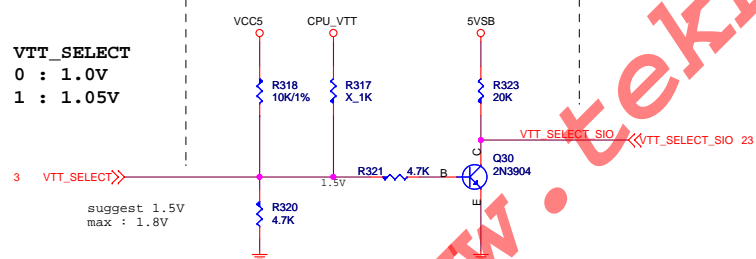
Iripple=2.55A



VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V

VTT_SELECT
0 : 1.0V
1 : 1.05V



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DDR Power:1.5V

DDR3_1.5V 4.75A+5.5A+0.5A=10.75A

4.75A FOR CPU

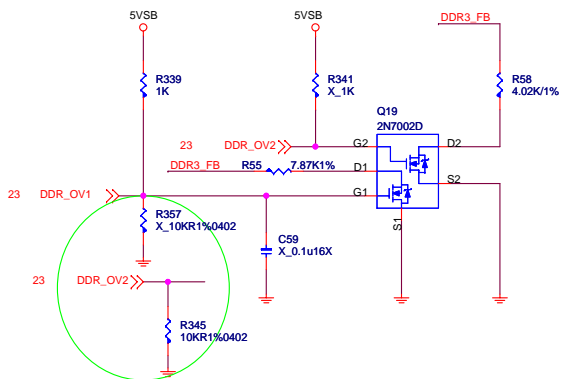
5.5A FOR 4DIMM

0.5A FOR DDR VTT

Tripple=4.868

$4.7*2*1=9.4A > 4.868A$

DDR OV

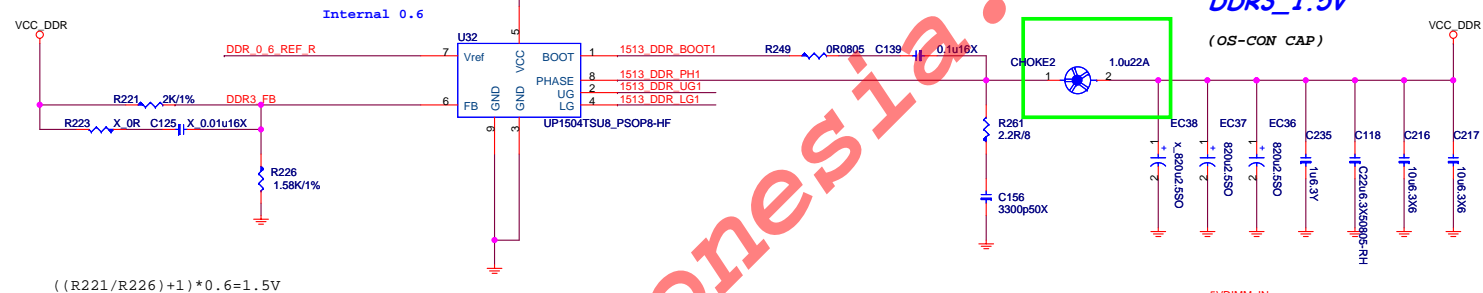


*Default 1.5V

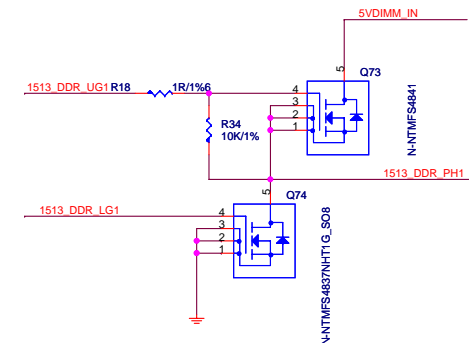
DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)

DDR_OV2 = GPIO02(S/IO)



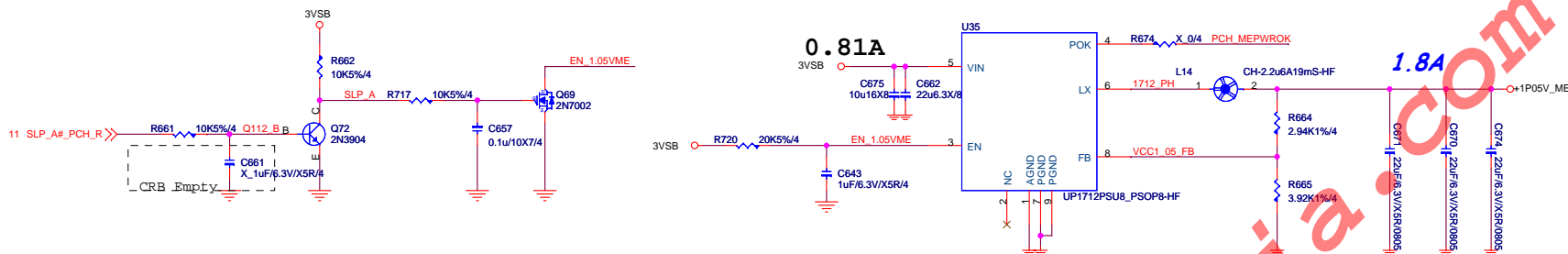
$((R221/R226)+1)*0.6=1.5V$



SLP_A

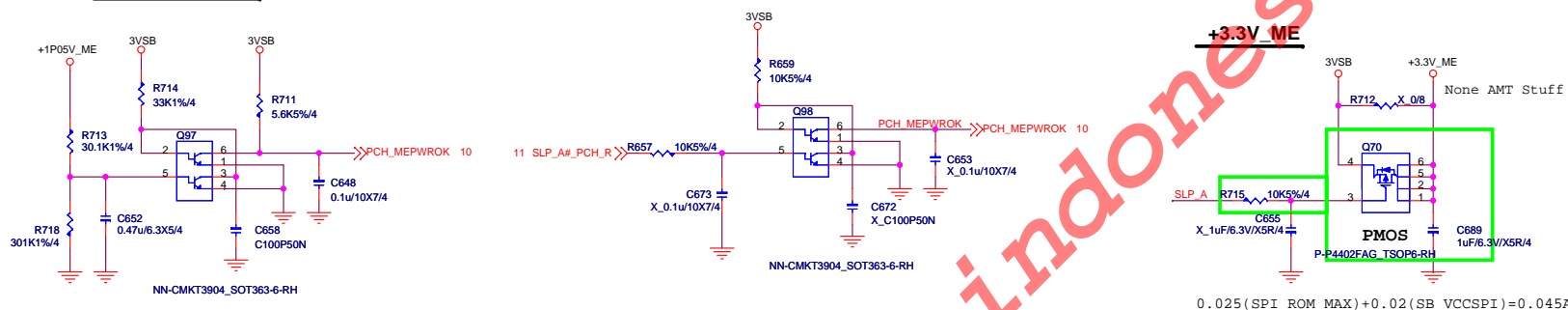
ME Power Control

+1.05V_ME(VCCIO_ME)

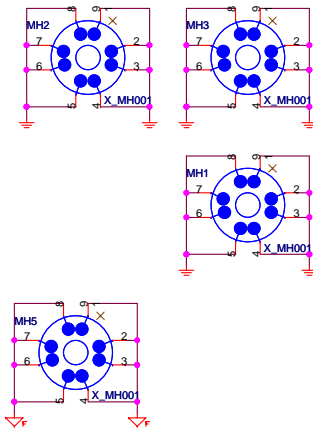


PCH_MEPWROK

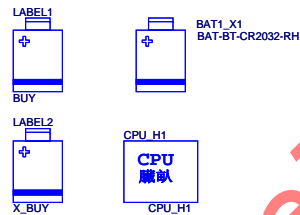
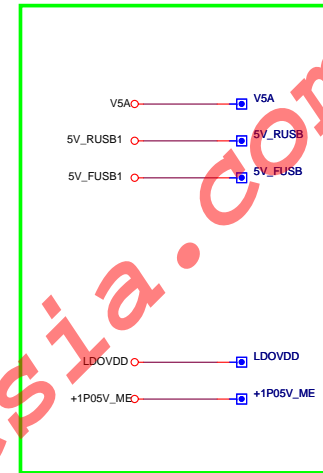
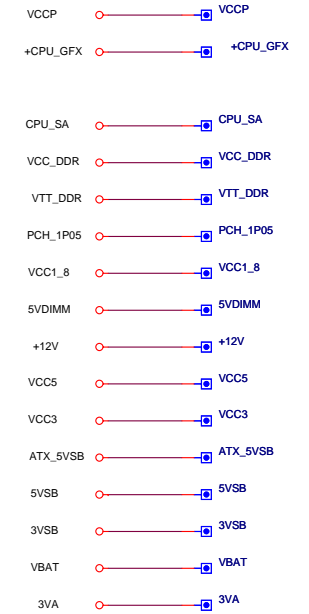
+3.3V_ME



Mounting Holes



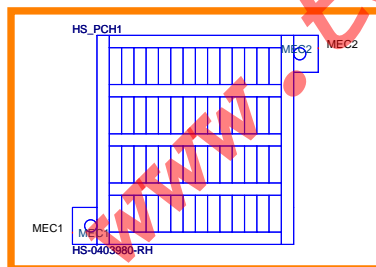
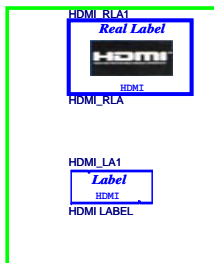
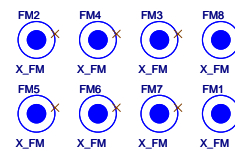
Voltage test point



Simulation



Optical Fiducial Marks-120




EMI:cap. for signal return path

EMI

EMI

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